


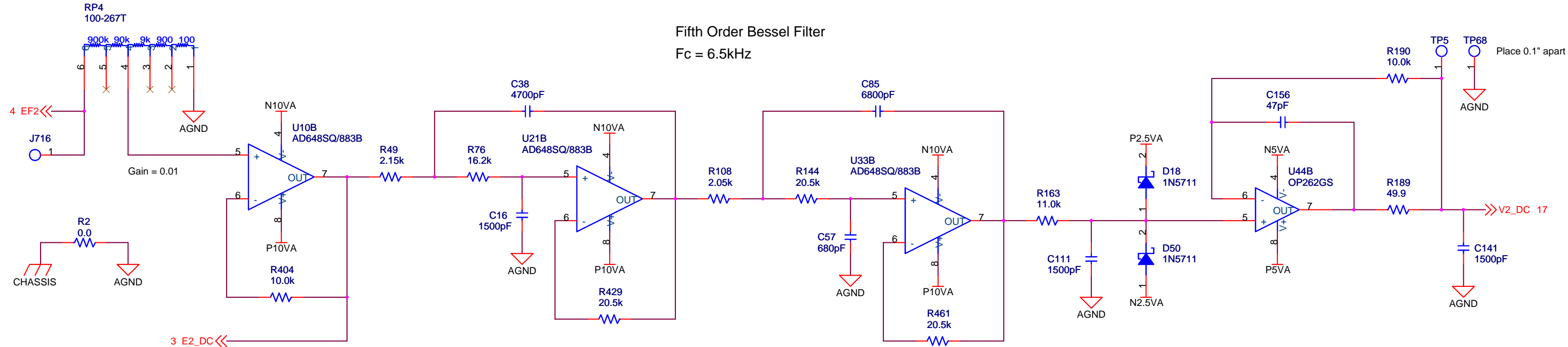
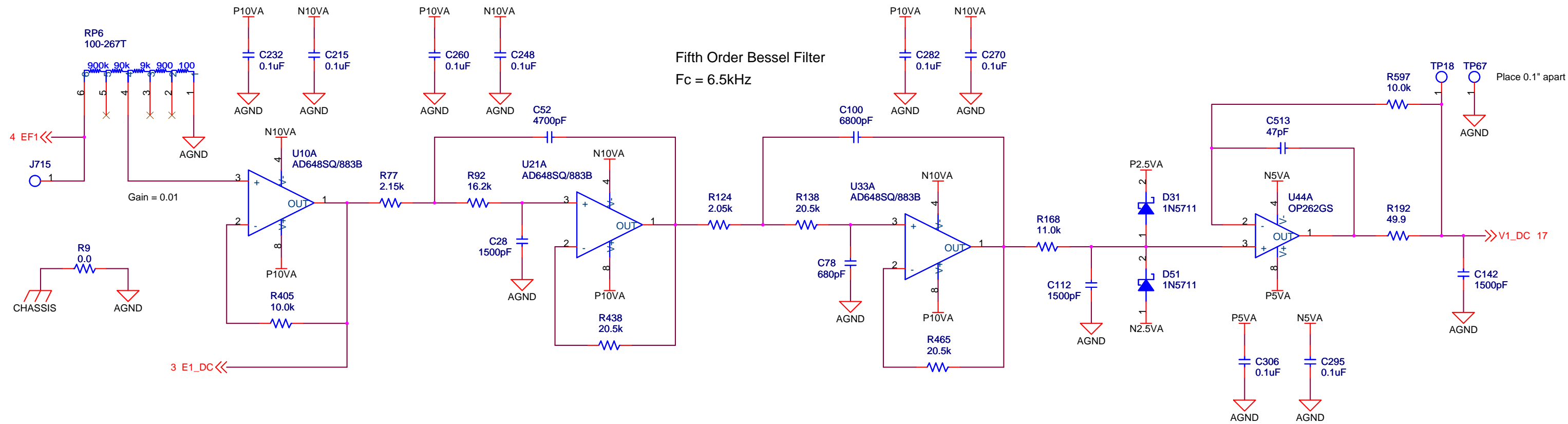
**GENERAL NOTES UNLESS OTHERWISE SPECIFIED:**

1) All screw holes shall be plated through holes with copper lands tied to Chassis\_Ground.

DNP = Do Not Populate component in this location

PROJECT CREATED: Monday, August 25, 2003		 <b>University of Colorado</b> <b>LASP Engineering Division</b> 1234 Innovation Drive Boulder, CO 80303						
PROJECT LAST MODIFIED Friday, November 19, 2010								
SCHEMATIC PAGE LAST MODIFIED Tuesday, November 16, 2010								
CONTRACT NO:<Contract Number>		SCALE: None	SHEET 1 of 27	SIZE: B				
USE (CHECK ONE)-----> 'X' denotes req'd signature		ASSEMBLY: EFW DFB						
CHECKED		SUBSYSTEM:						
		FLT PRT	FLT ASM	NON FLT	GSE	<b>Schematic Diagram</b> PART NO: <b>110947</b>		
Assembly		X	X					
Engineer		X	X	X	X	TITLE <b>EFW Digital Fields Board</b>		
ME			X					
EE		X	X		X	PROJECT: <b>EFW DFB</b>		
Thermal			X					
System			X		X	REV. <b>D</b>		
QA / CM		X	X		X			
FILE NAME: C:\LASP_SVN\PROJECTS\FIELDS\TRUNK\EFW\DFB\PWAFMPCB\SCH\LASP110947_EFW_DFB_SCHEMATIC_REV.DSN								

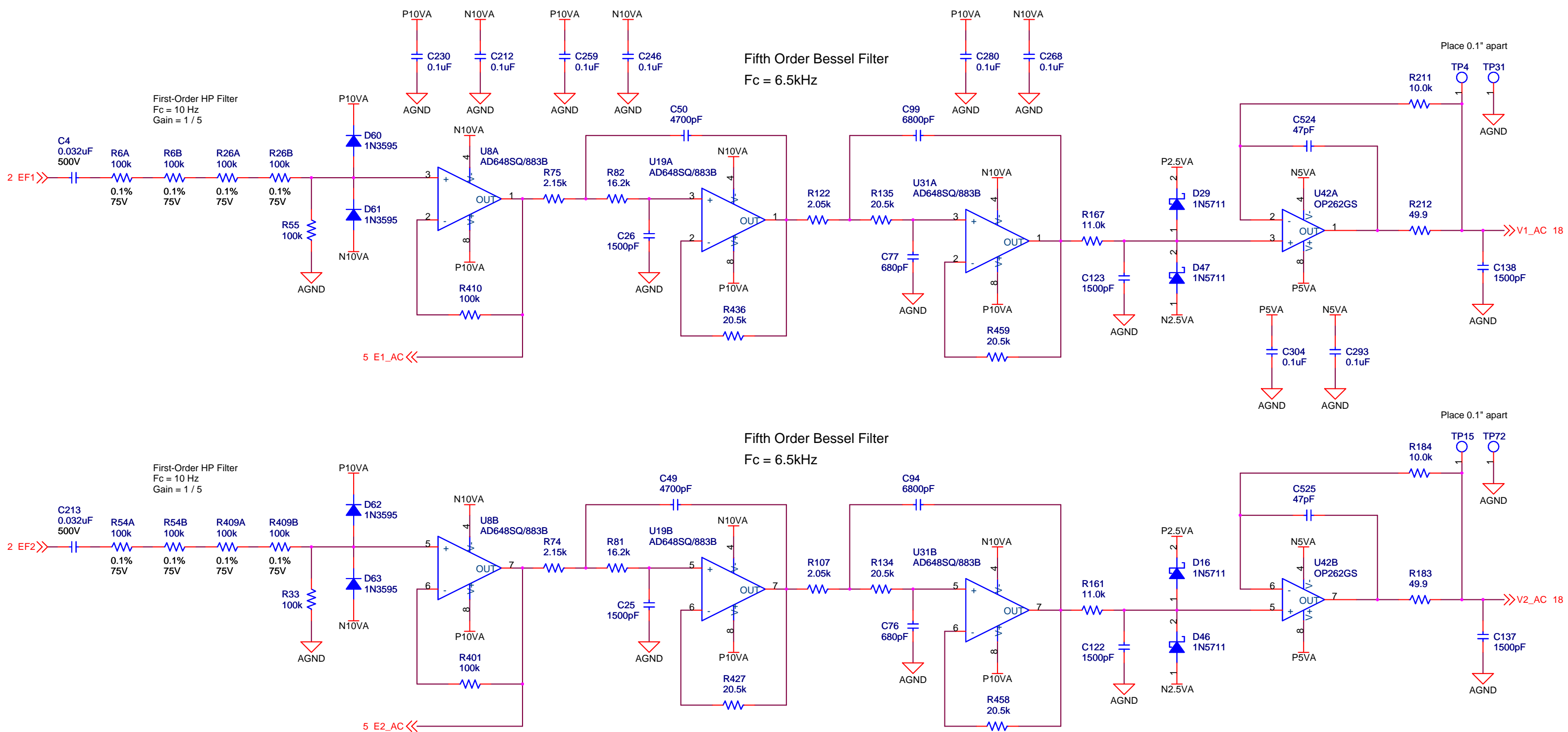
### V1 and V2 DC-Coupled Lowpass Filters



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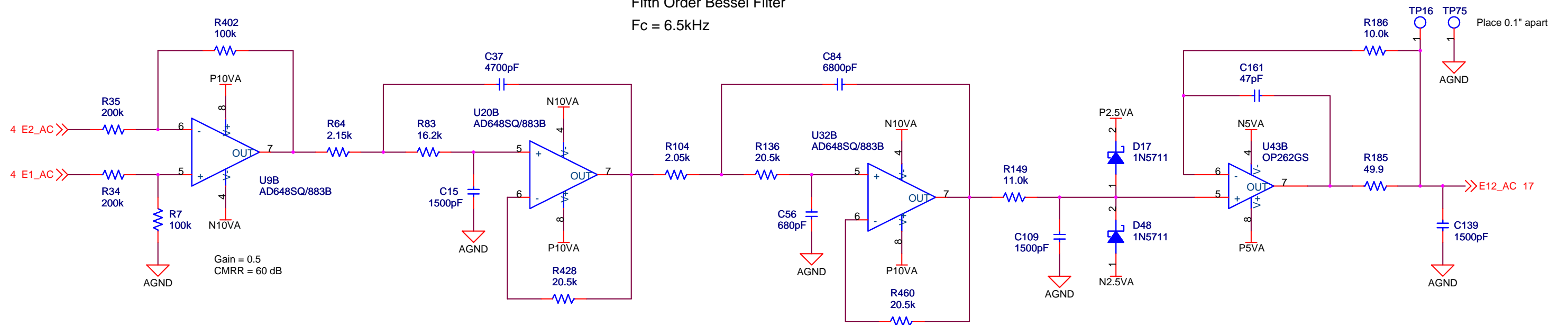
# V1 and V2 AC-Coupled Bandpass Filter for Solitary Wave Detector



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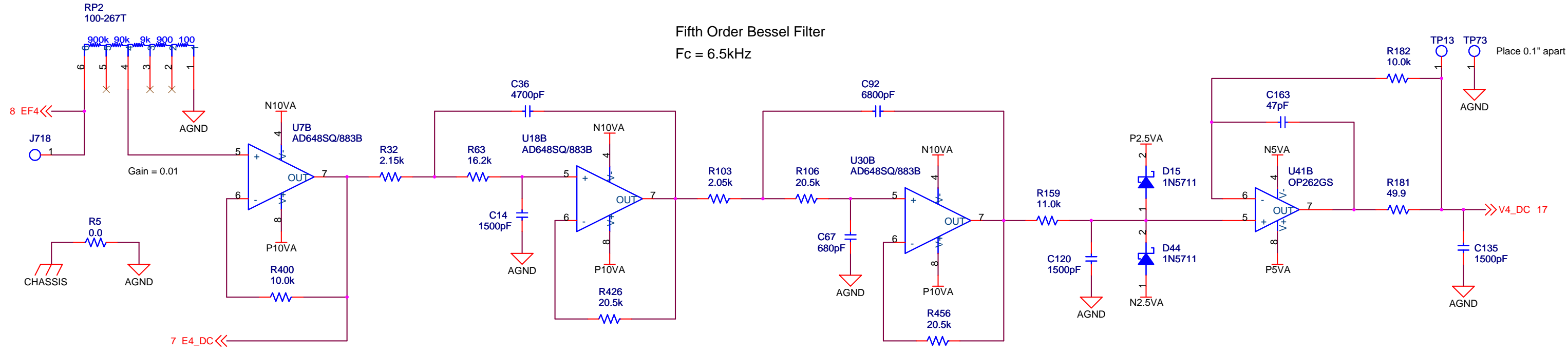
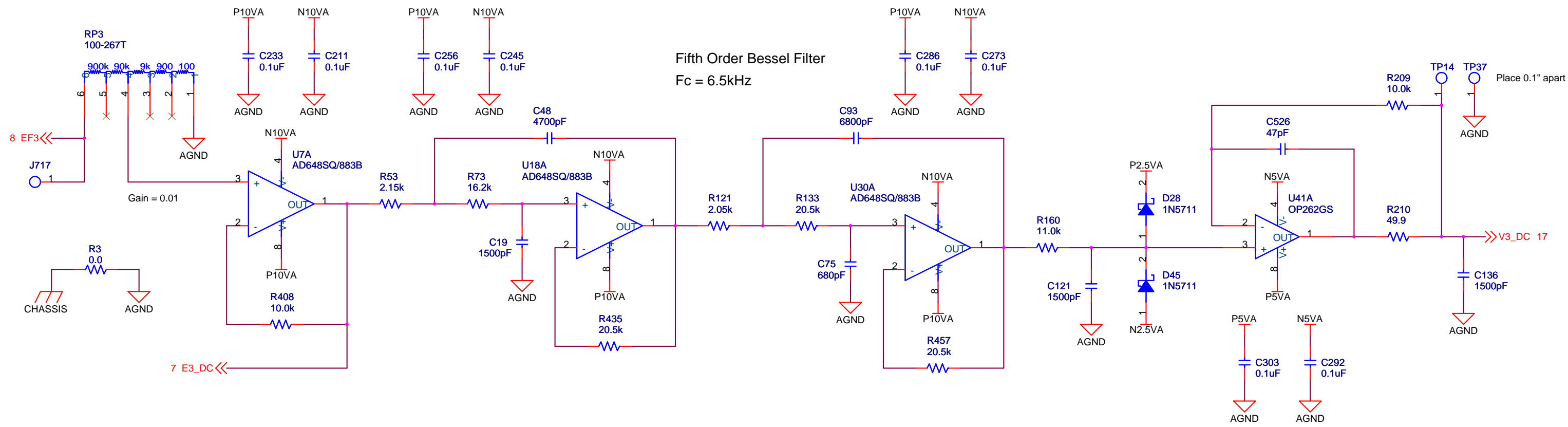
# E12 AC-Coupled Bandpass Filter

Fifth Order Bessel Filter  
 $F_c = 6.5\text{kHz}$



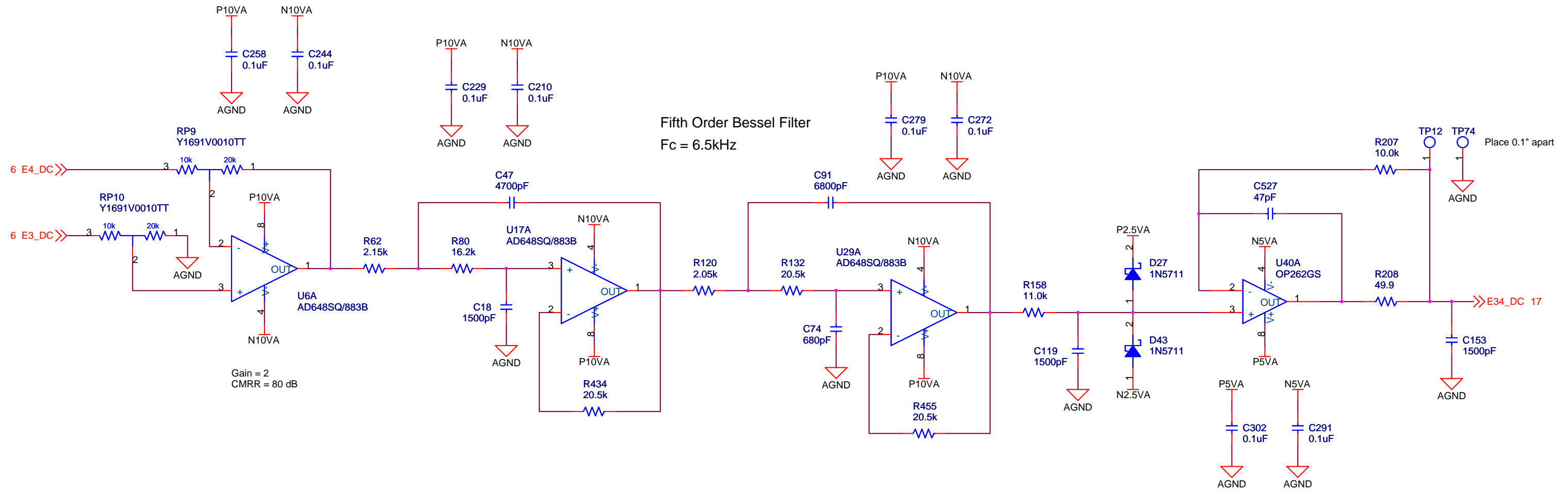
Title		
EFW Digital Fields Board		
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### V3 and V4 DC-Coupled Lowpass Filters



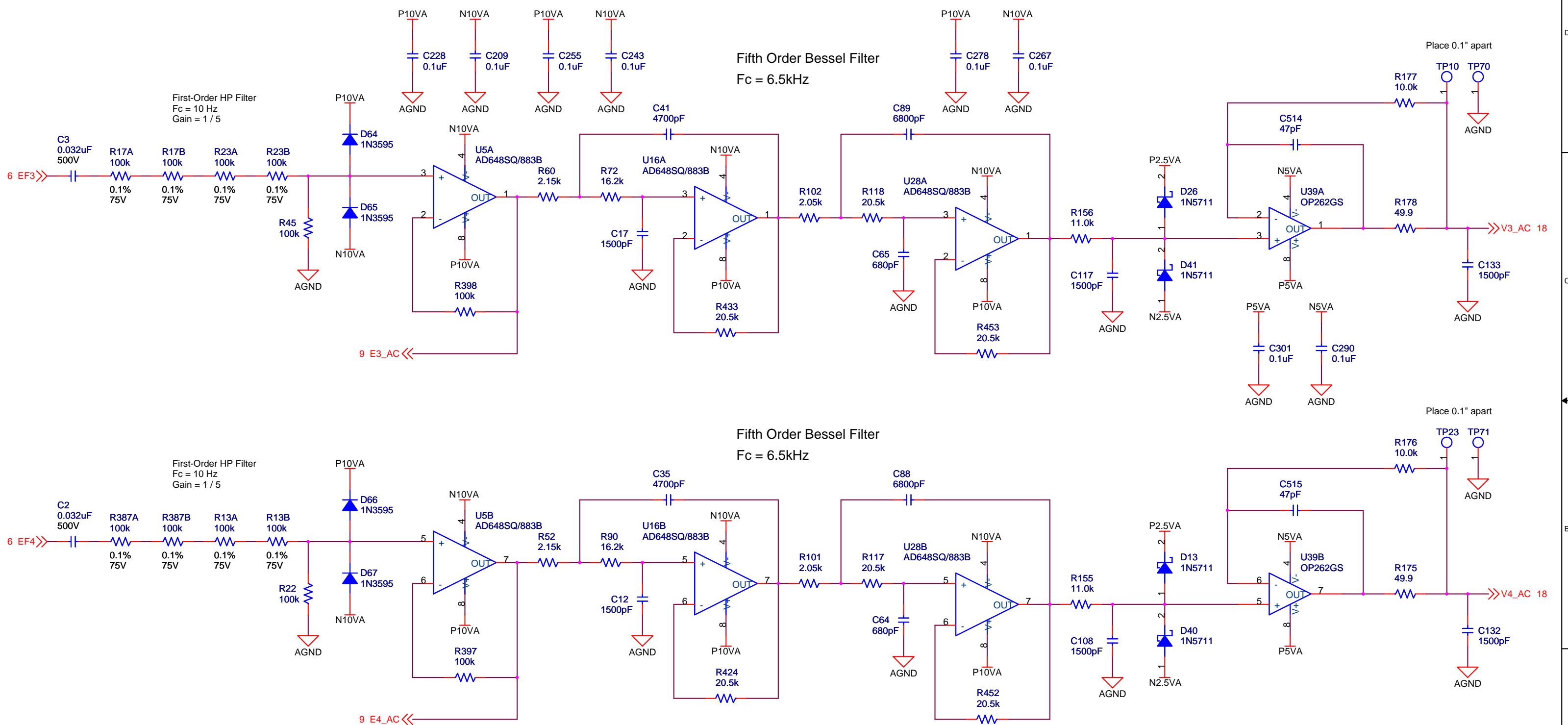
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EFW Digital Fields Board		
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# E34 DC-Coupled Lowpass Filter



Title		
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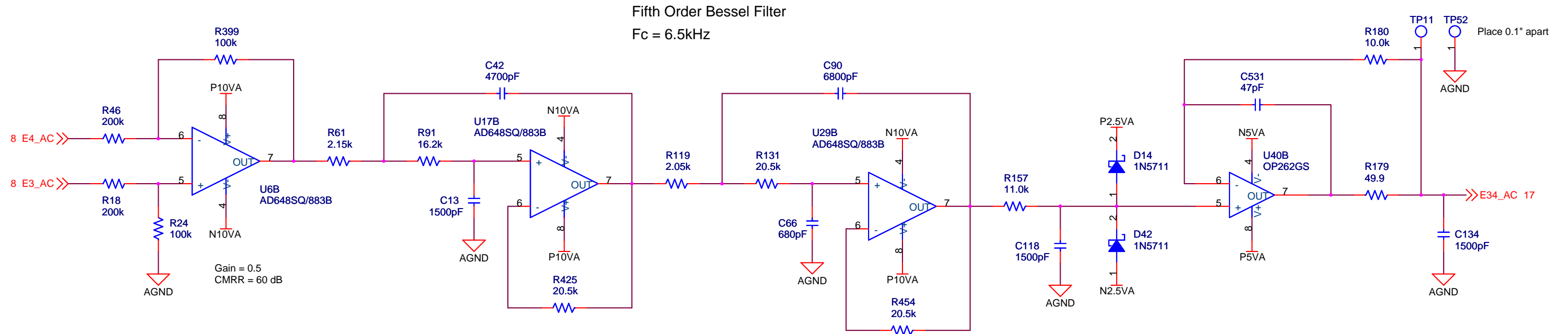
### V3 and V4 AC-Coupled Bandpass Filter for Solitary Wave Detector



Title		
EFW Digital Fields Board		
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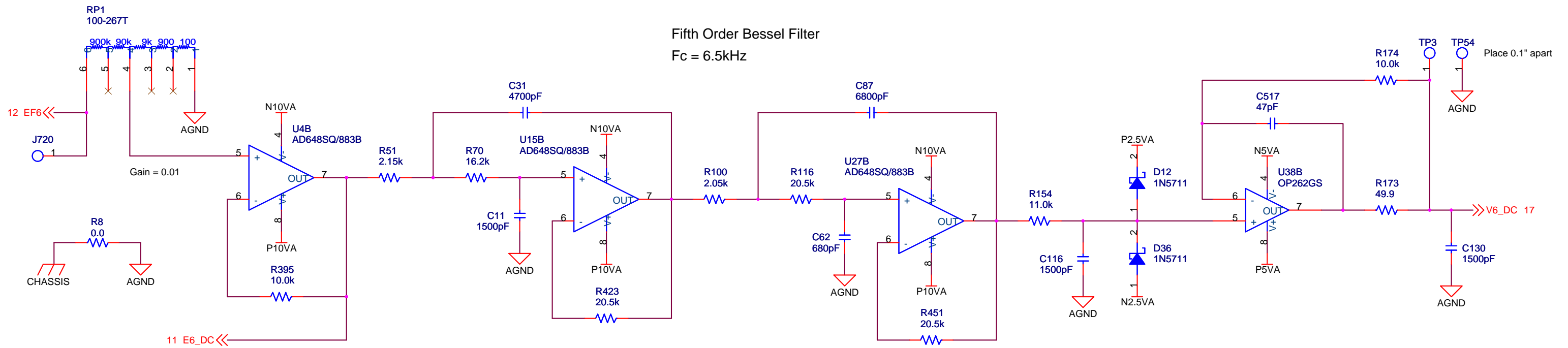
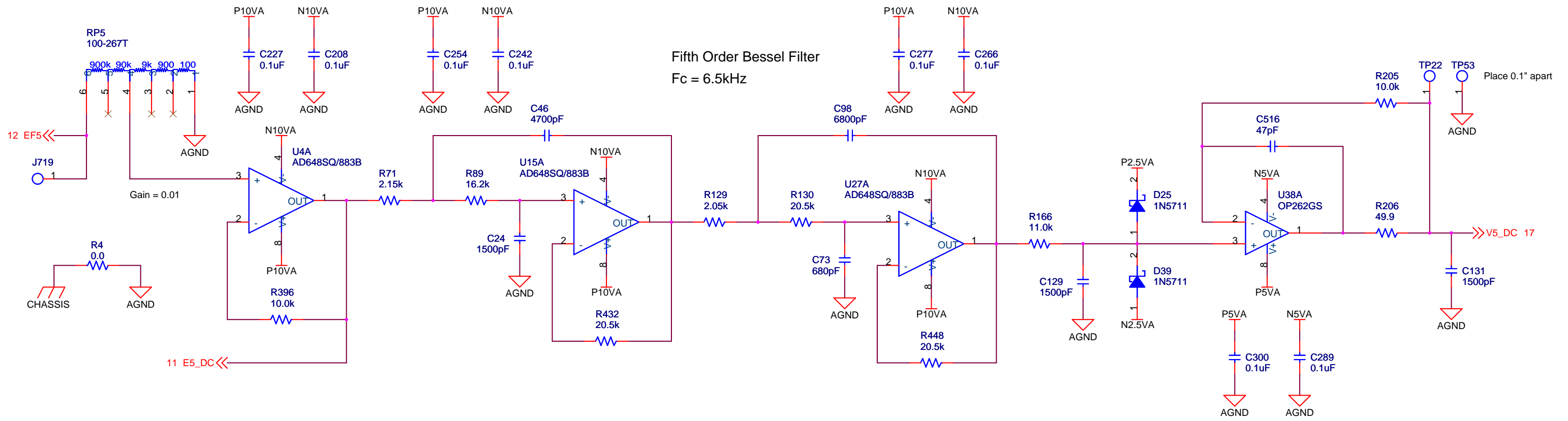


# E34 AC-Coupled Bandpass Filter



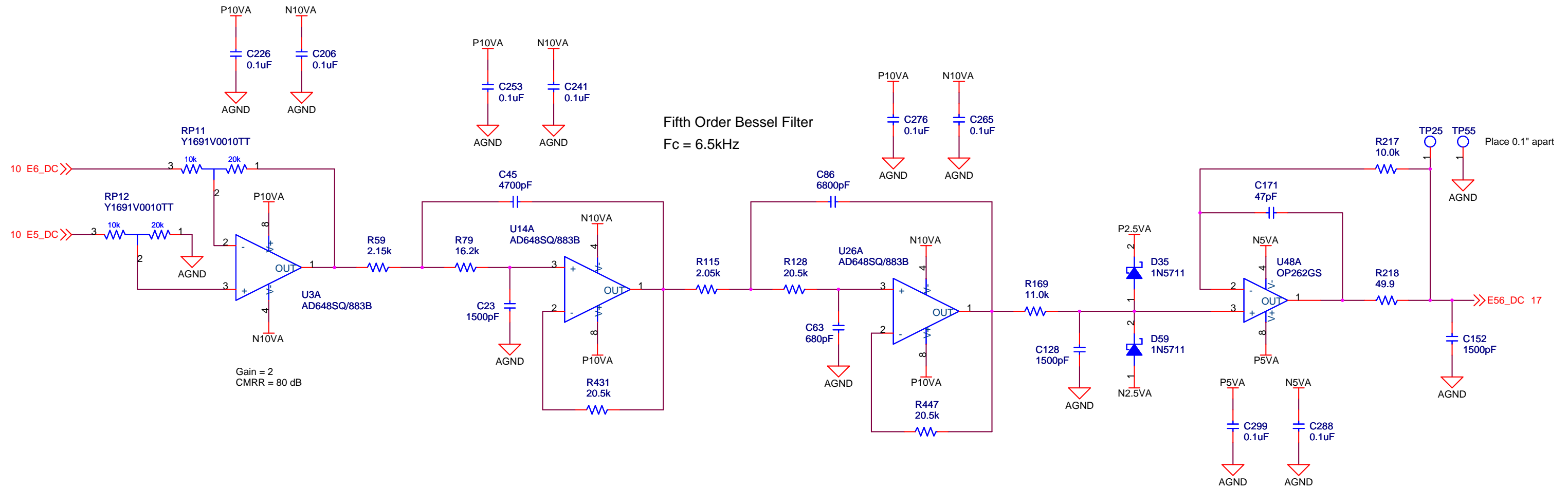
Title		
EFW Digital Fields Board		
Size	Document Number	Rev
B	110947	D
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### V5 and V6 DC-Coupled Lowpass Filters



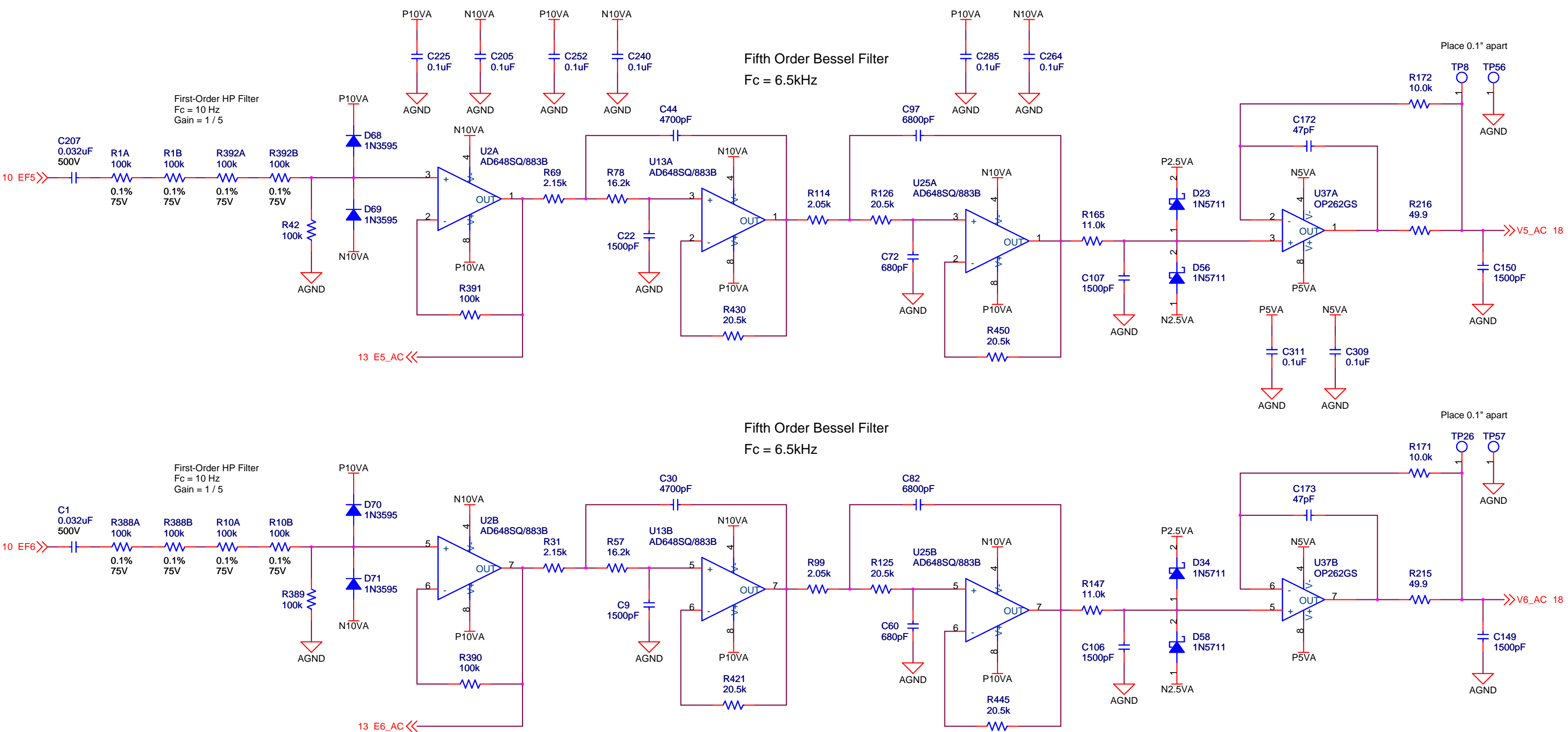
Title		
EFW Digital Fields Board		
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# E56 DC-Coupled Lowpass Filter



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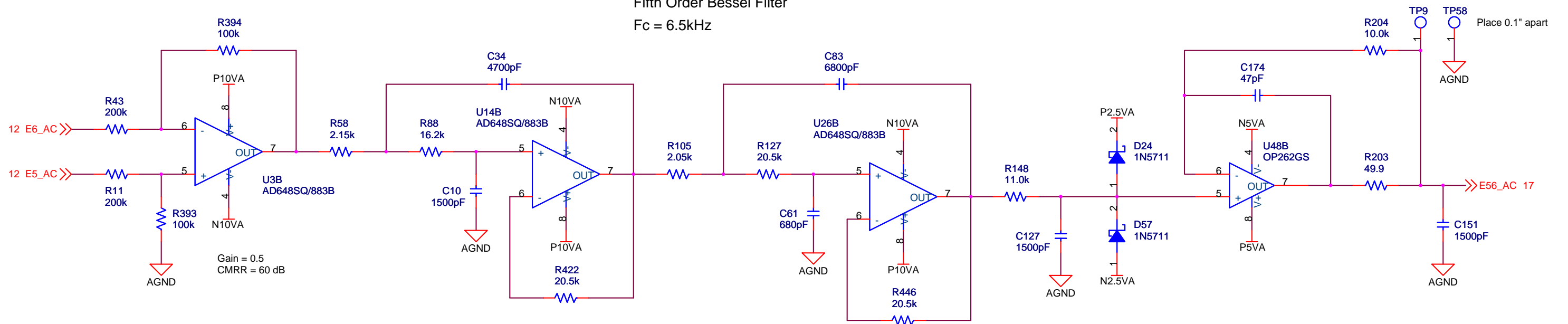
# V5 and V6 AC-Coupled Bandpass Filter for Solitary Wave Detector



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# E56 AC-Coupled Bandpass Filter

Fifth Order Bessel Filter  
 $F_c = 6.5\text{kHz}$

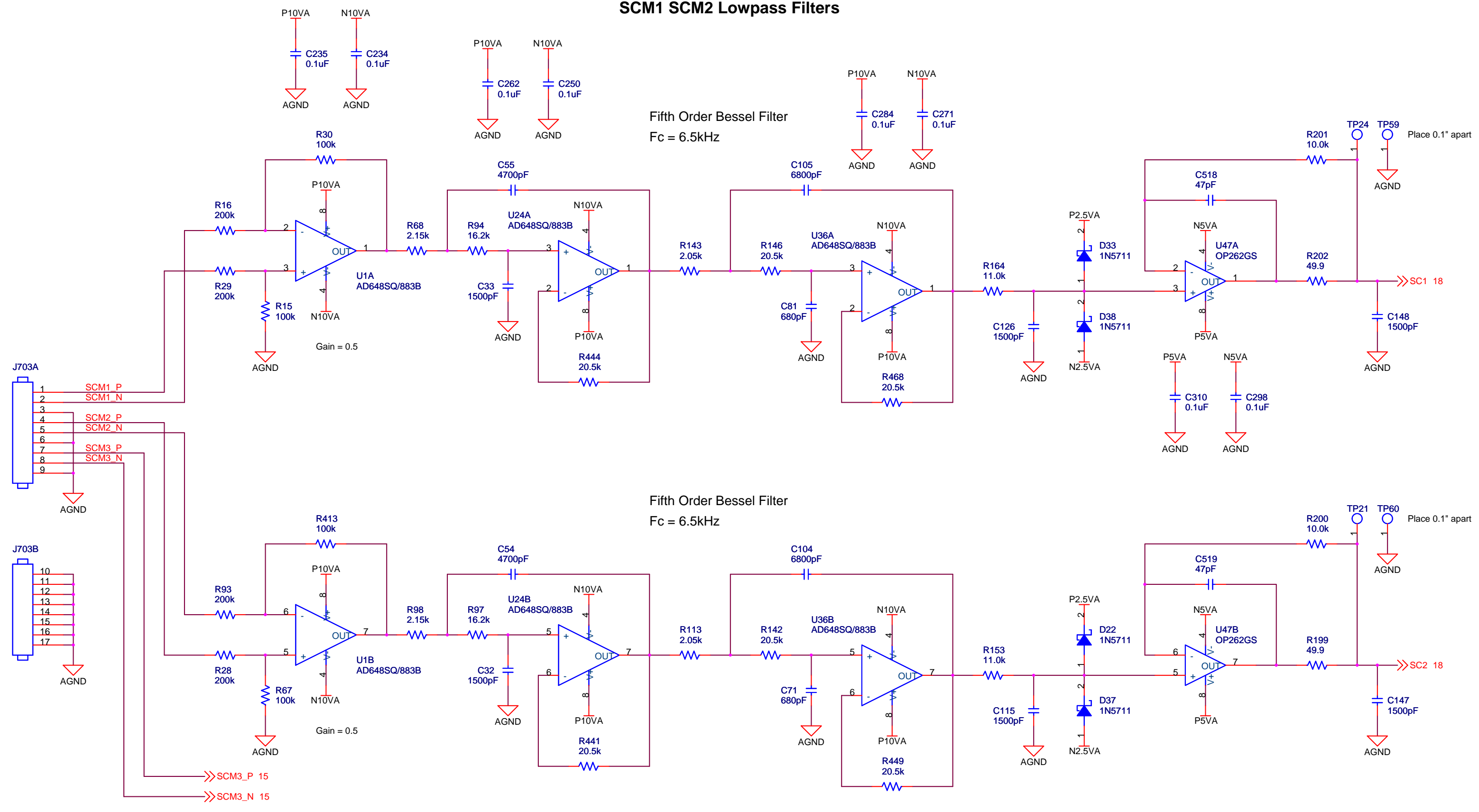


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### SCM1 SCM2 Lowpass Filters

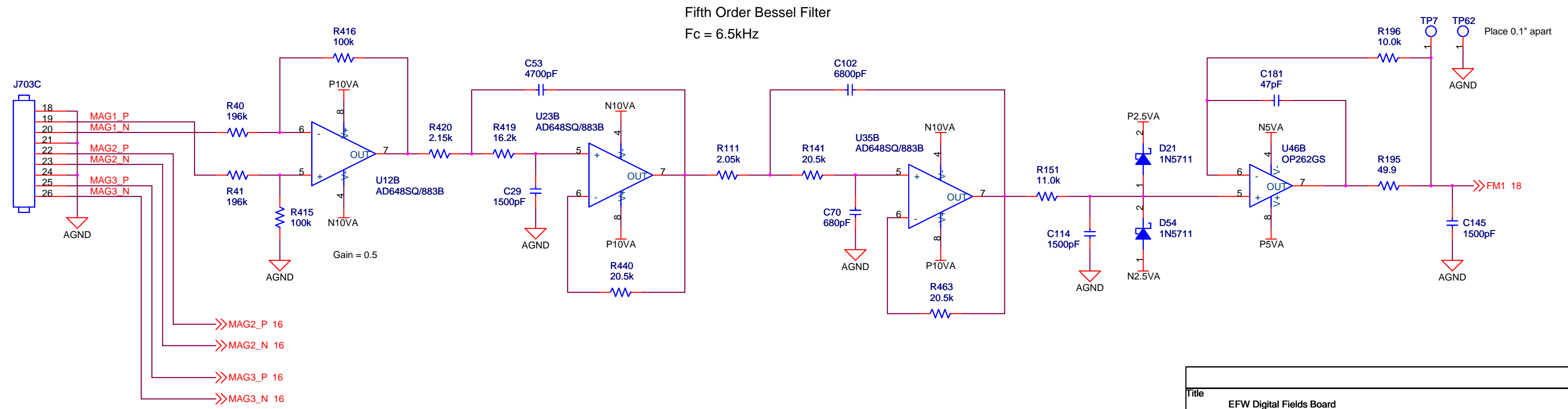
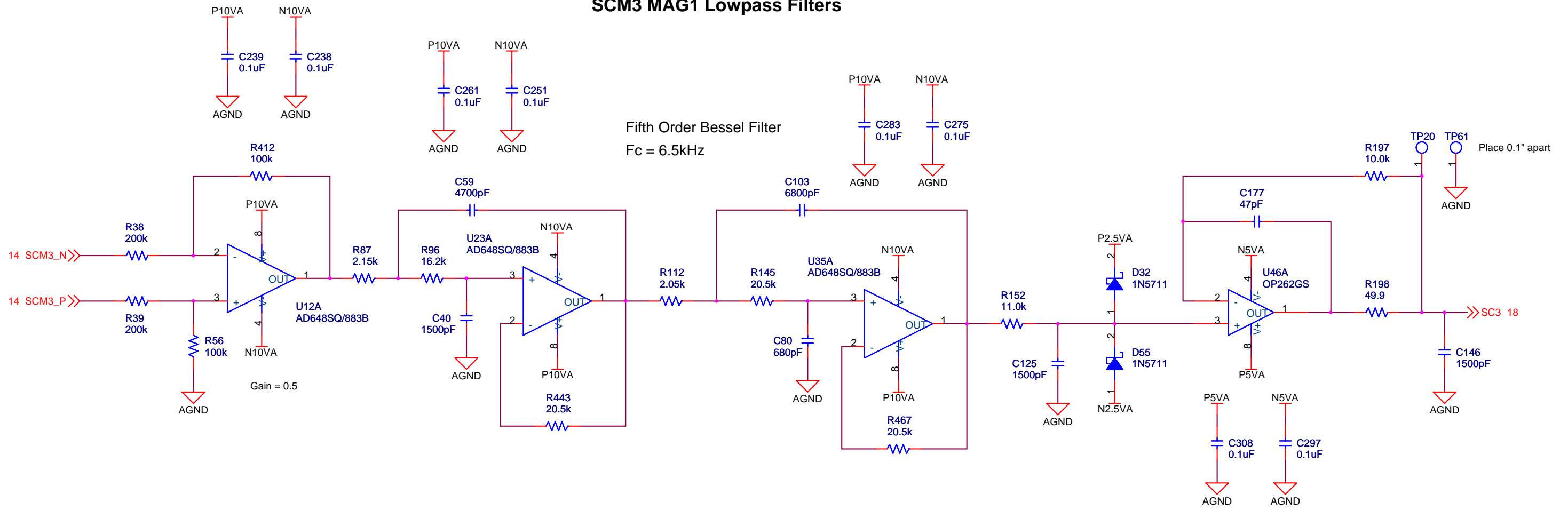
Fifth Order Bessel Filter  
 $F_c = 6.5\text{kHz}$

Fifth Order Bessel Filter  
 $F_c = 6.5\text{kHz}$



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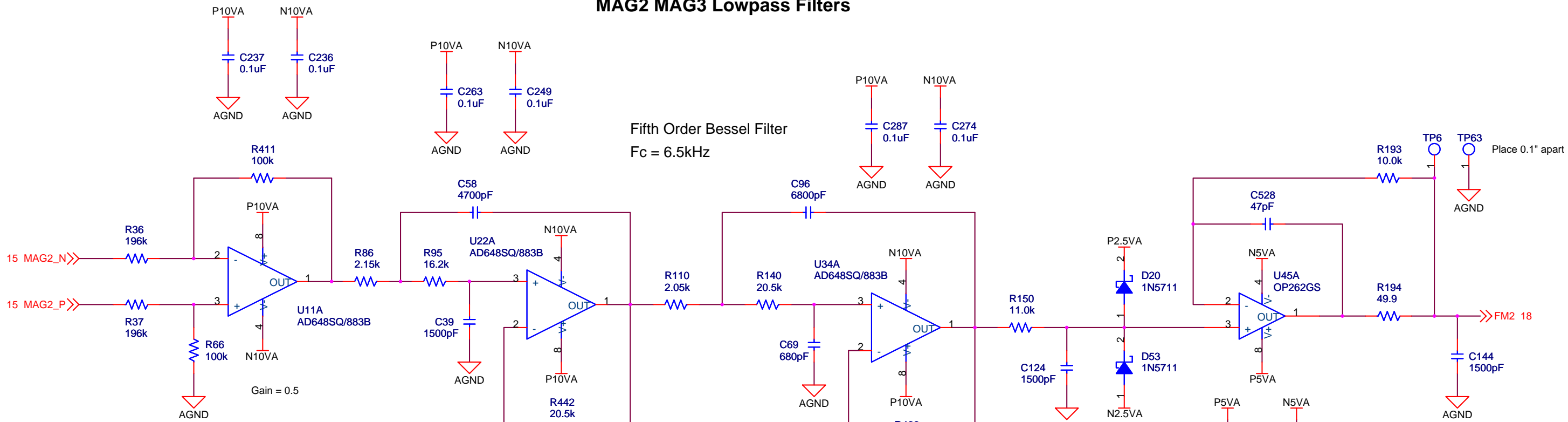
### SCM3 MAG1 Lowpass Filters



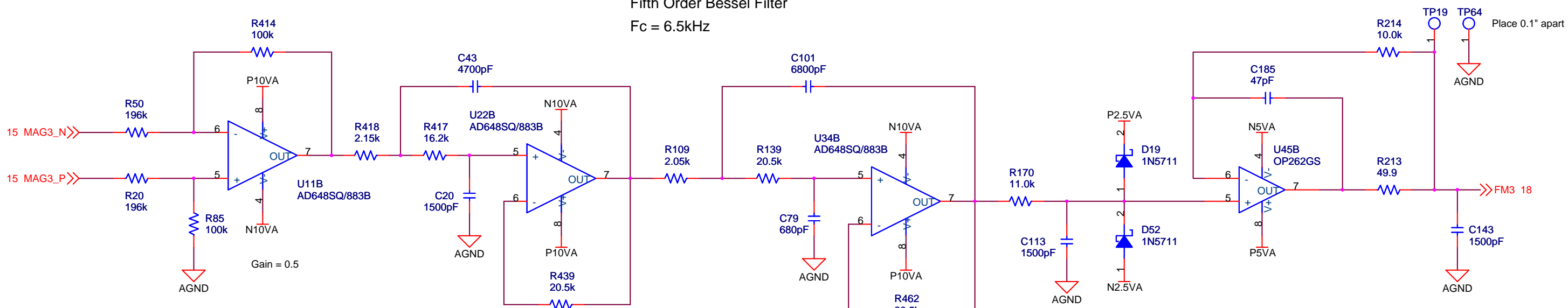
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EFW Digital Fields Board		
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### MAG2 MAG3 Lowpass Filters

Fifth Order Bessel Filter  
 $F_c = 6.5\text{kHz}$



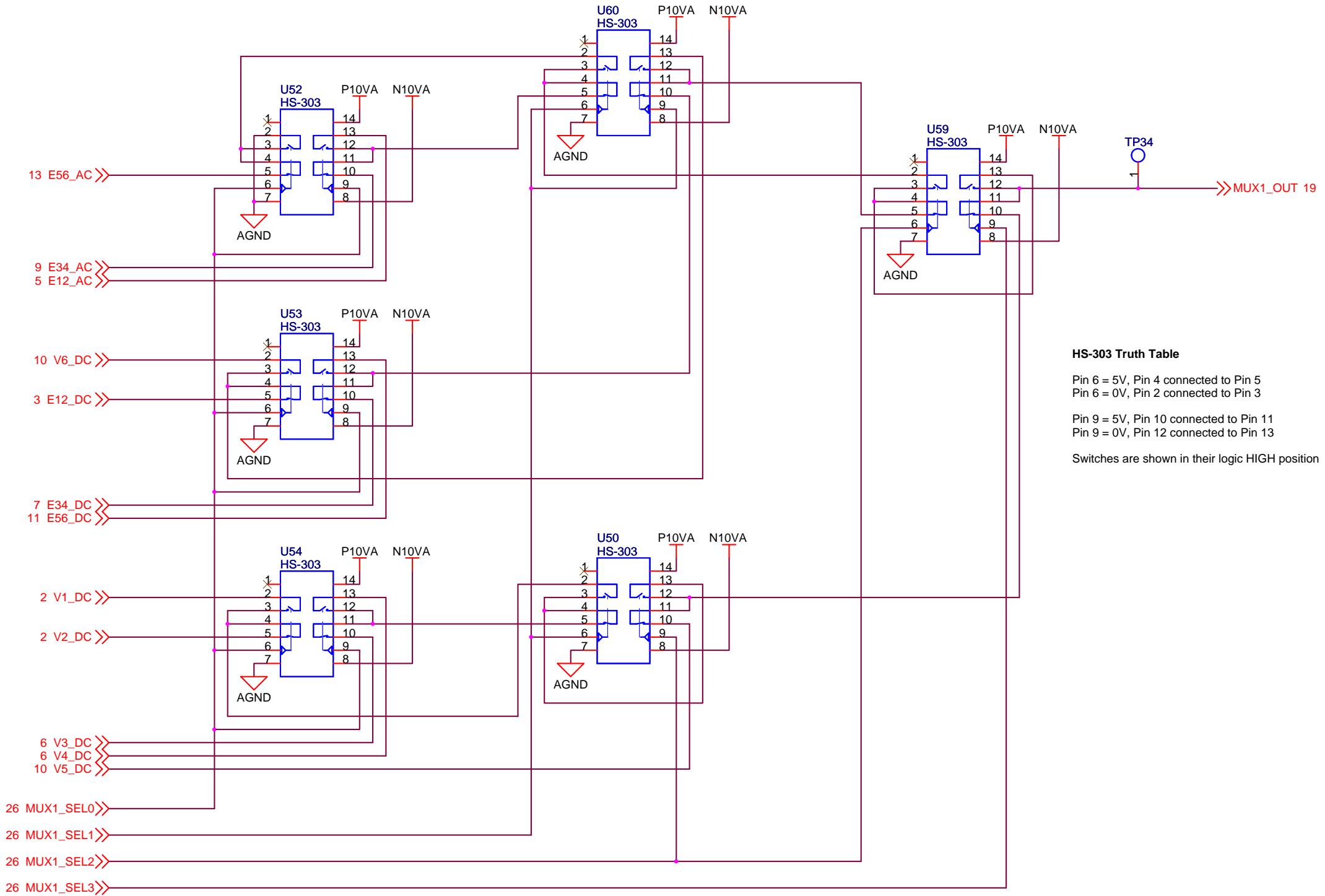
Fifth Order Bessel Filter  
 $F_c = 6.5\text{kHz}$



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# Analog Multiplexer 1



### HS-303 Truth Table

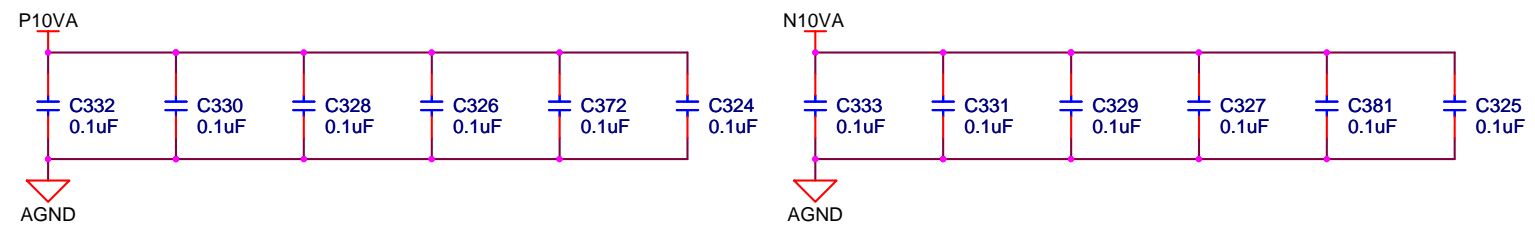
Pin 6 = 5V, Pin 4 connected to Pin 5  
 Pin 6 = 0V, Pin 2 connected to Pin 3

Pin 9 = 5V, Pin 10 connected to Pin 11  
 Pin 9 = 0V, Pin 12 connected to Pin 13

Switches are shown in their logic HIGH position

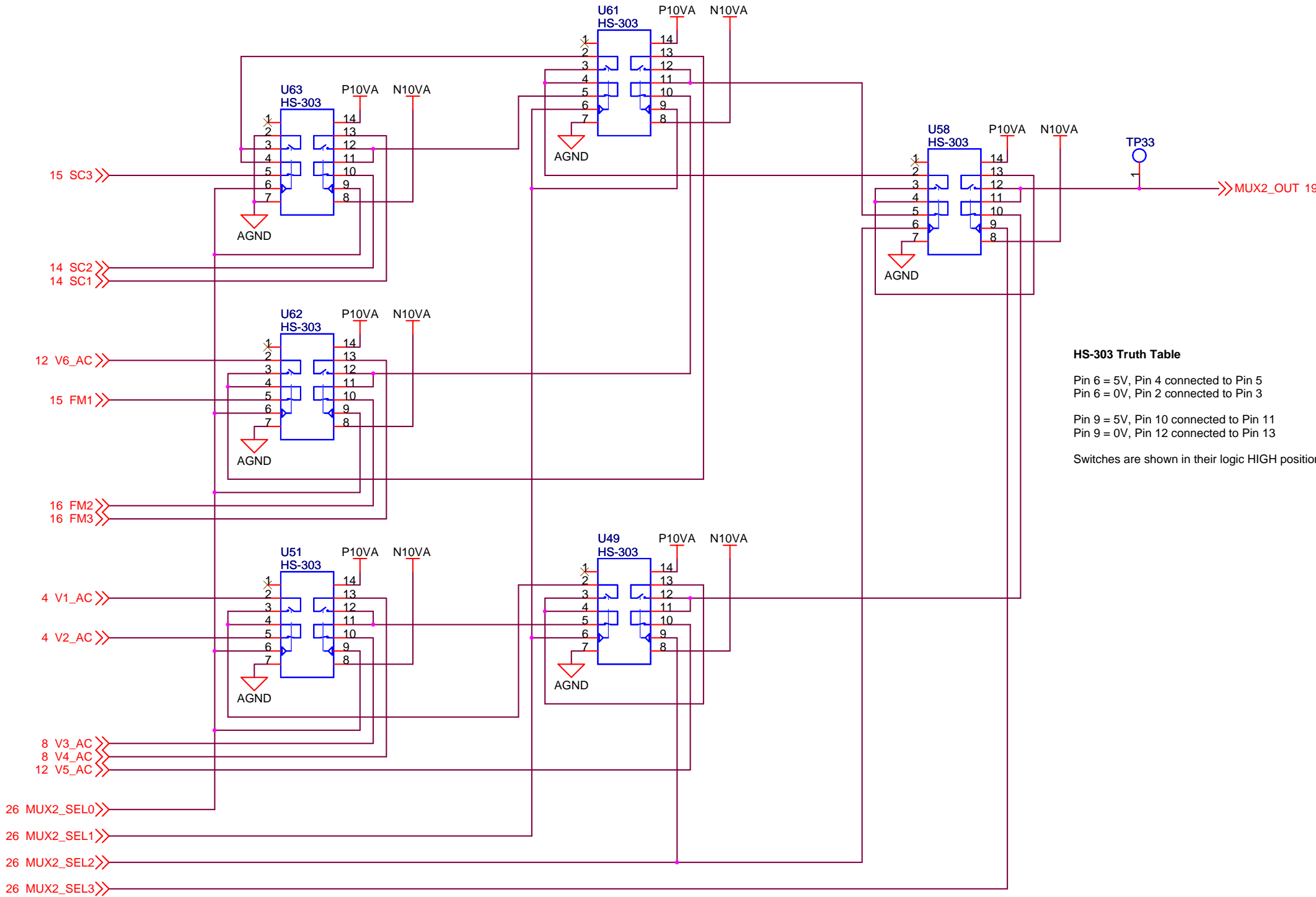
Channel	MUX1_SEL(3:0)
V1_DC	1000
V2_DC	1001
V3_DC	1011
V4_DC	1010
V5_DC	1110
V6_DC	0100
E12_DC	0101
E34_DC	0111
E56_DC	0110
E12_AC	0010
E34_AC	0011
E56_AC	0001
AGND	0000

Note: Channels are ordered so that the addresses are grey-coded binary. This minimizes the number of analog switches that switch at one time in order to reduce the settling time of the multiplexer



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EFW Digital Fields Board		
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# Analog Multiplexer 2



### HS-303 Truth Table

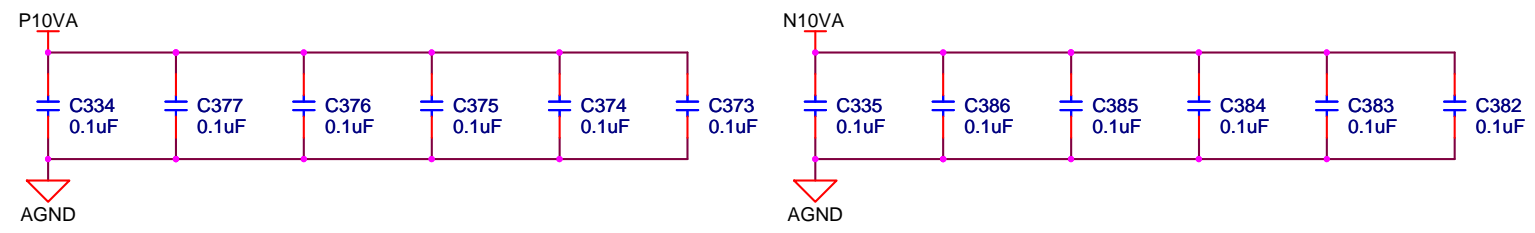
Pin 6 = 5V, Pin 4 connected to Pin 5  
 Pin 6 = 0V, Pin 2 connected to Pin 3

Pin 9 = 5V, Pin 10 connected to Pin 11  
 Pin 9 = 0V, Pin 12 connected to Pin 13

Switches are shown in their logic HIGH position

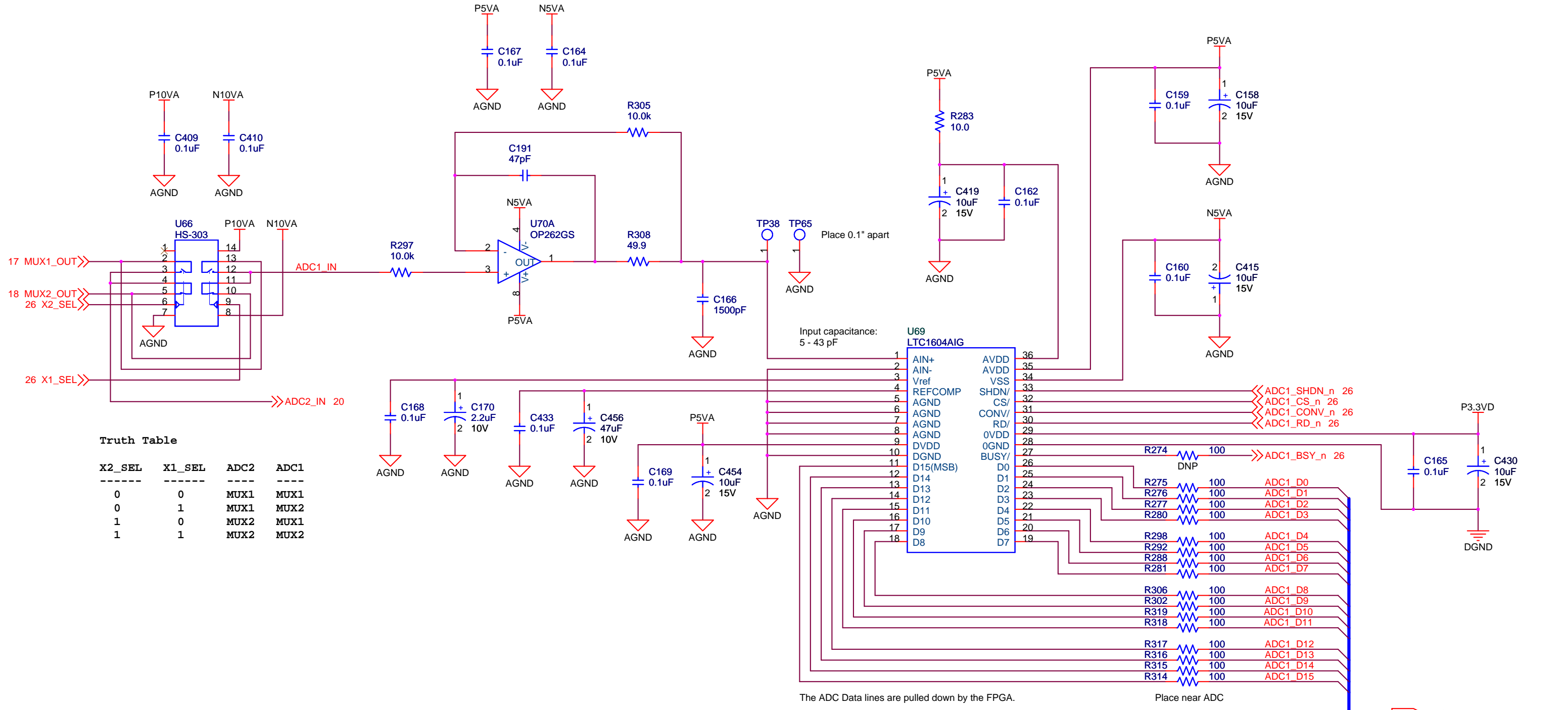
Channel	MUX2_SEL(3:0)
V1_AC	1000
V2_AC	1001
V3_AC	1011
V4_AC	1010
V5_AC	1110
V6_AC	0100
FM1	0101
FM2	0111
FM3	0110
SC1	0010
SC2	0011
SC3	0001
AGND	0000

Note: Channels are ordered so that the addresses are grey-coded binary. This minimizes the number of analog switches that switch at one time in order to reduce the settling time of the multiplexer



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# ADC 1



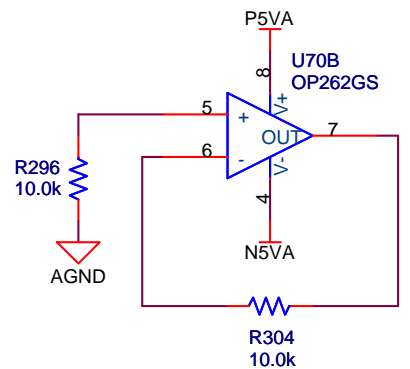
Truth Table

X2_SEL	X1_SEL	ADC2	ADC1
0	0	MUX1	MUX1
0	1	MUX1	MUX2
1	0	MUX2	MUX1
1	1	MUX2	MUX2

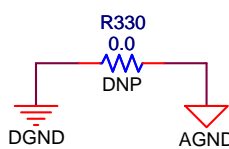
The ADC Data lines are pulled down by the FPGA.

Place near ADC

Place near ADC 1



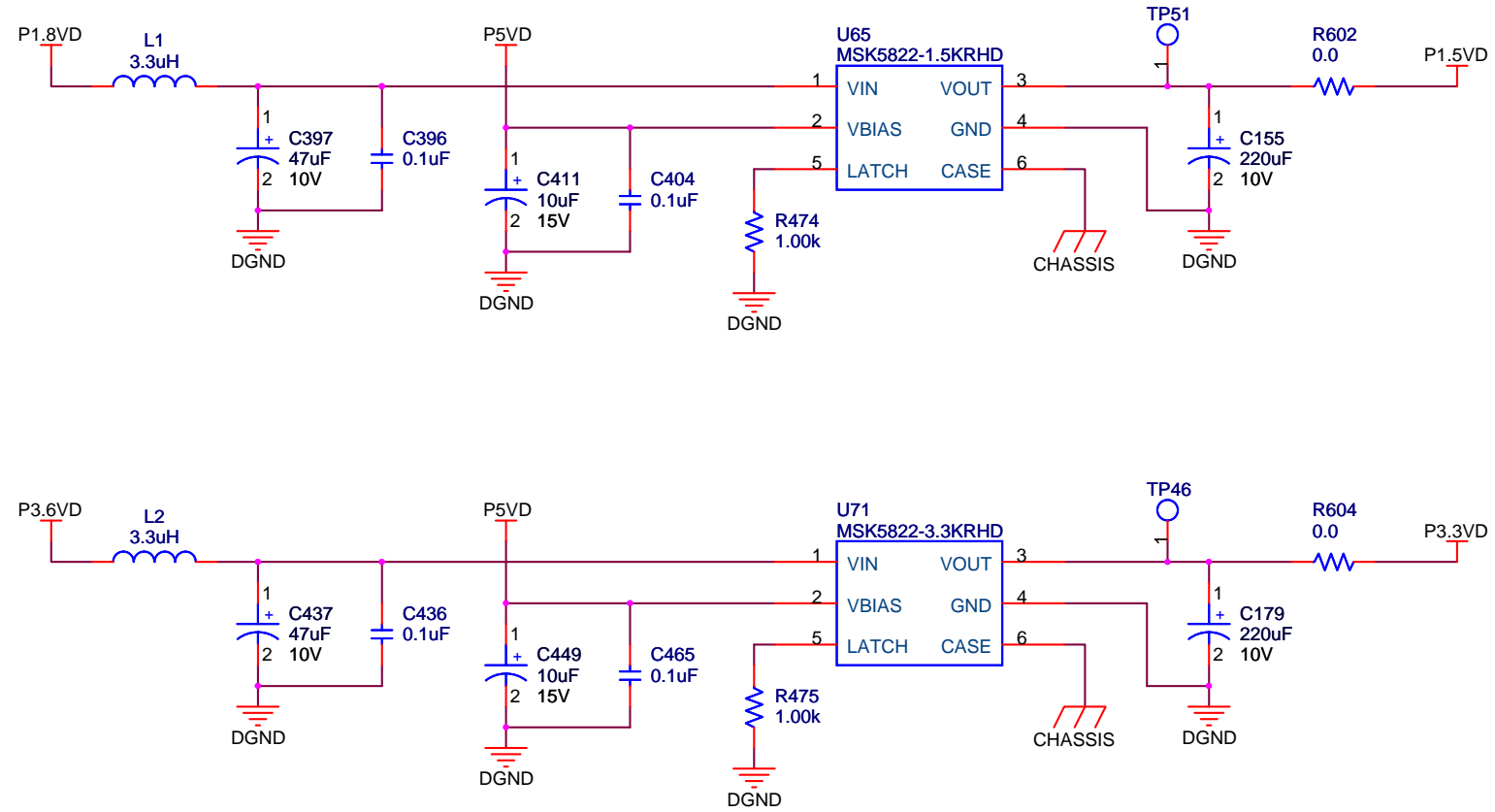
Unused Op-amp



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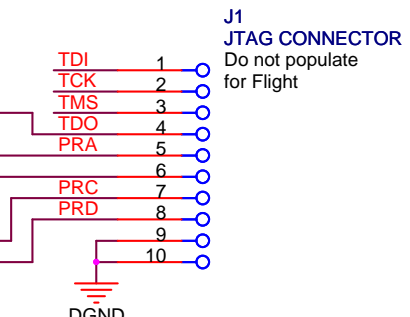
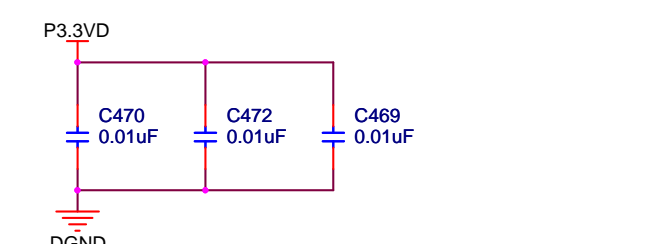
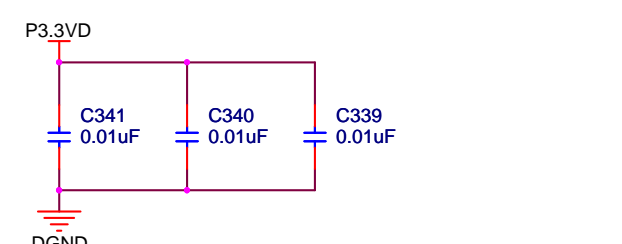
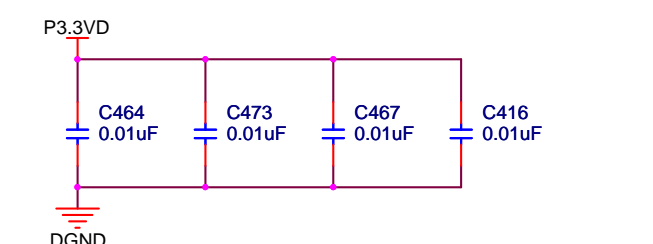
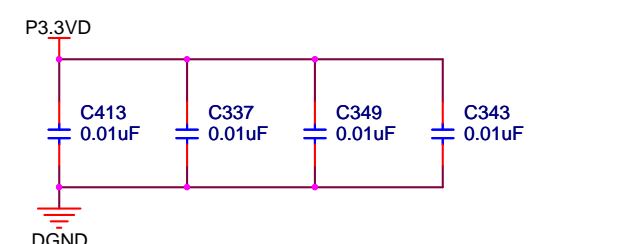
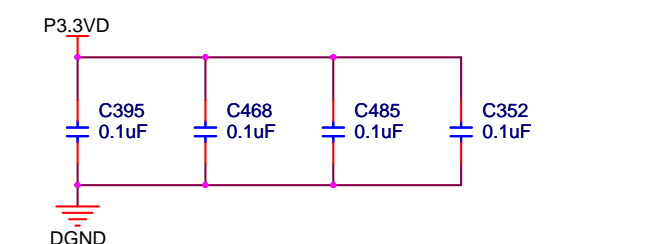
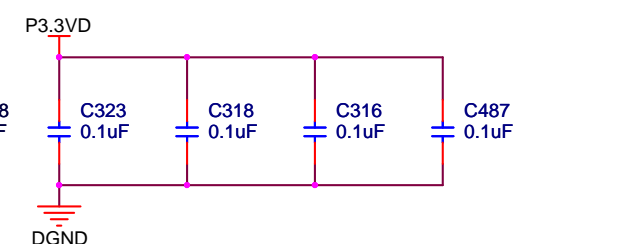
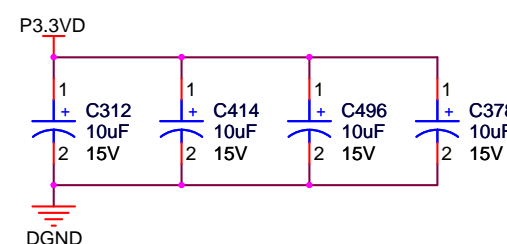
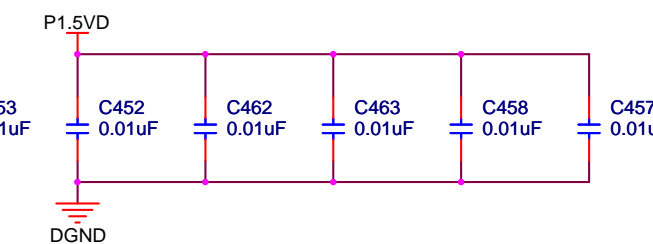
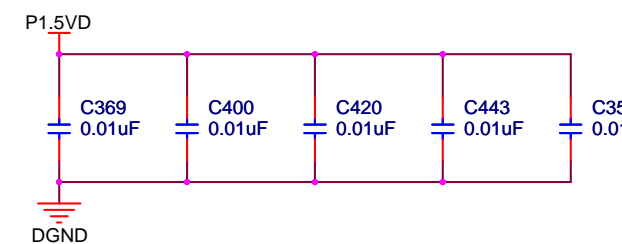
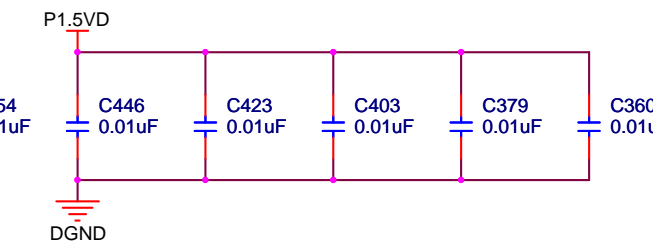
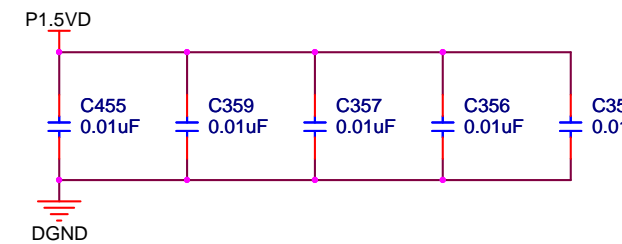
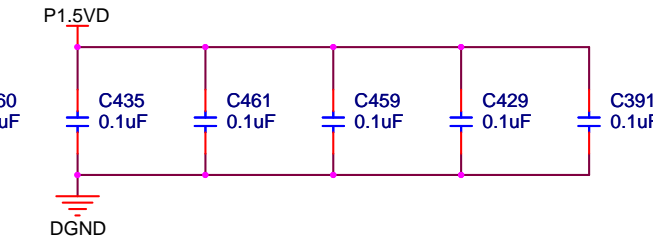
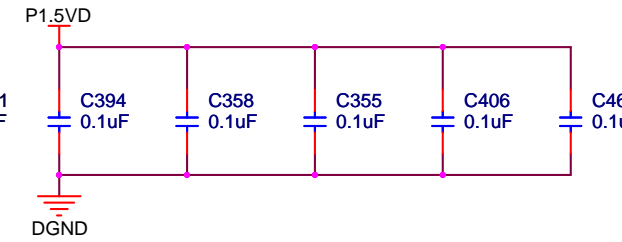
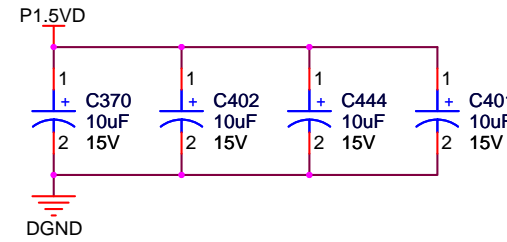
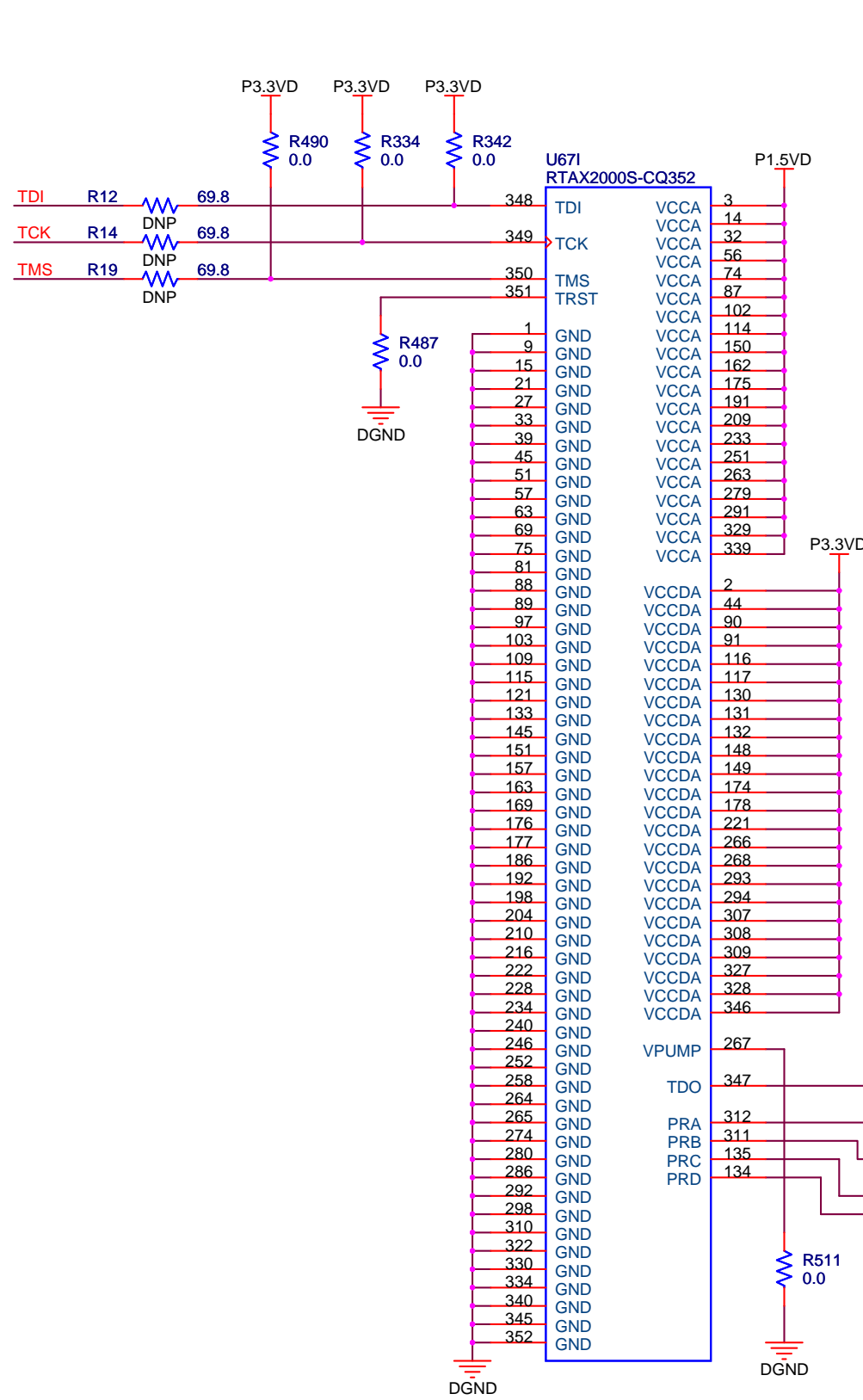


# FPGA Voltage Regulators



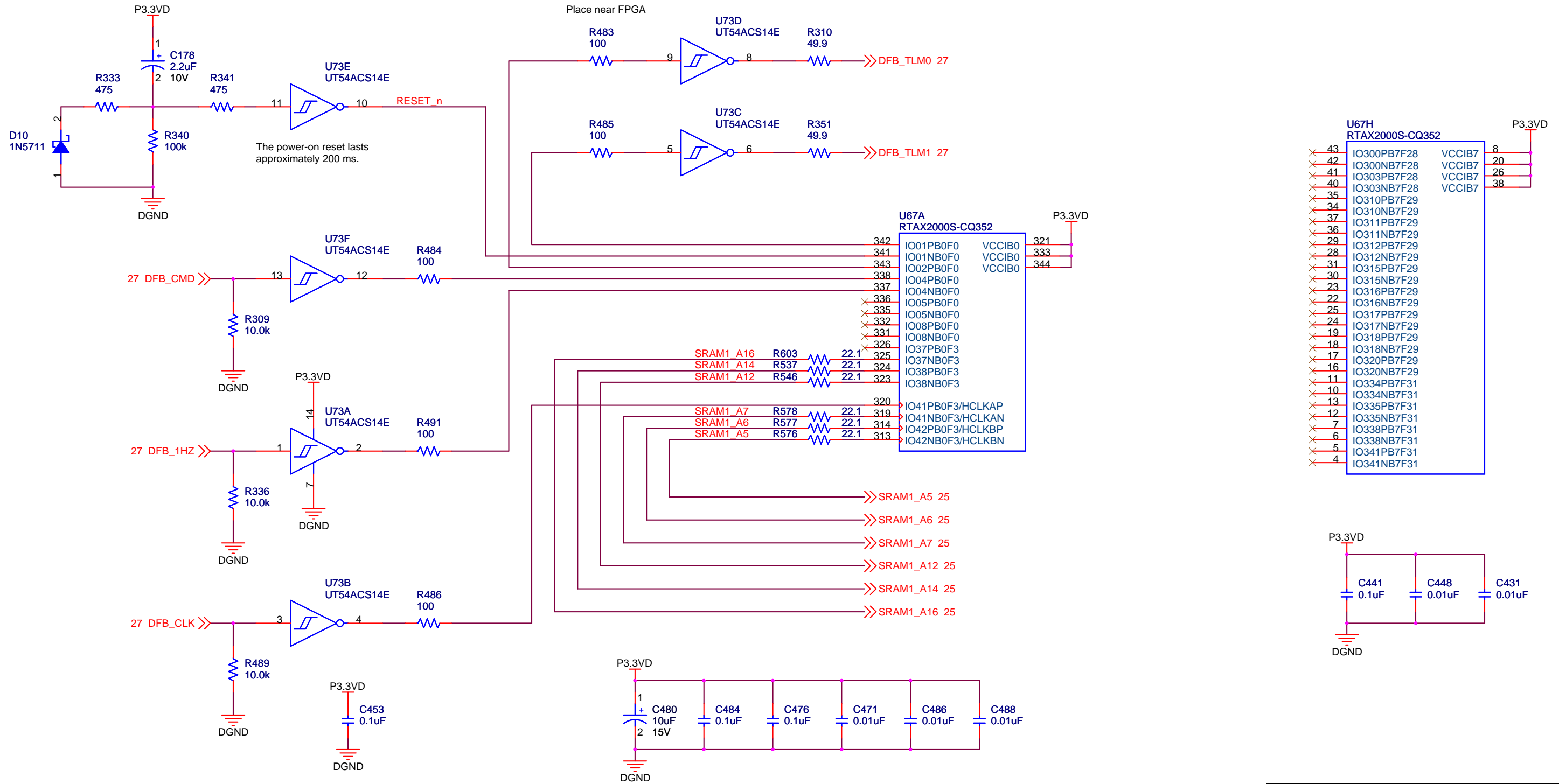
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# FPGA Power and JTAG



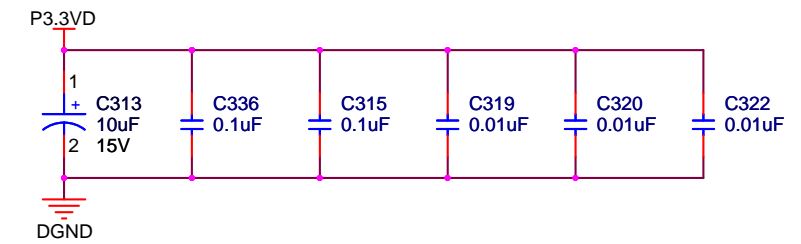
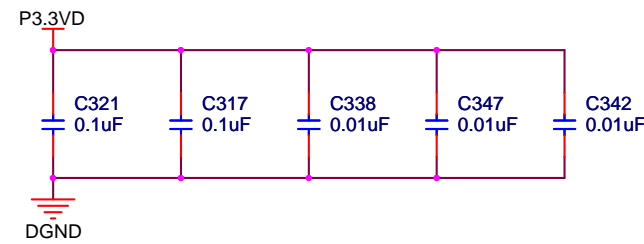
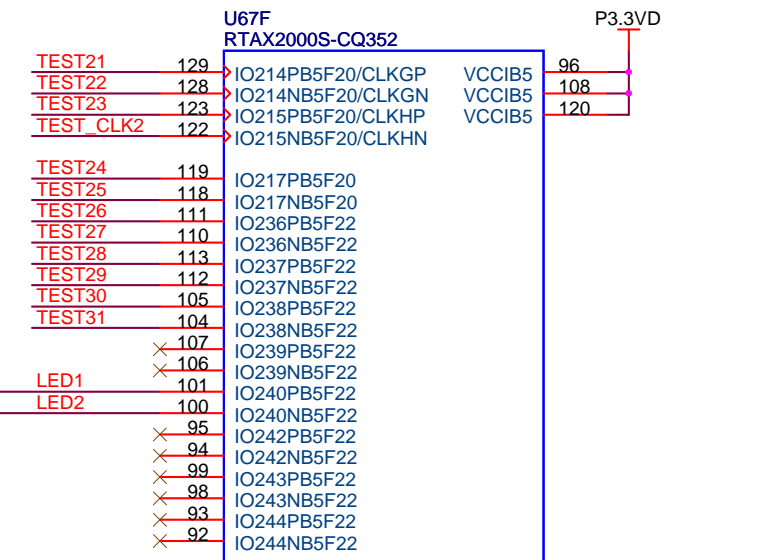
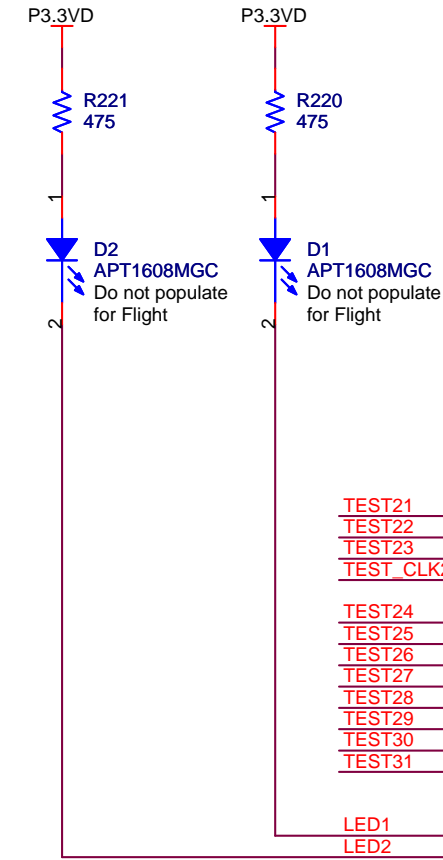
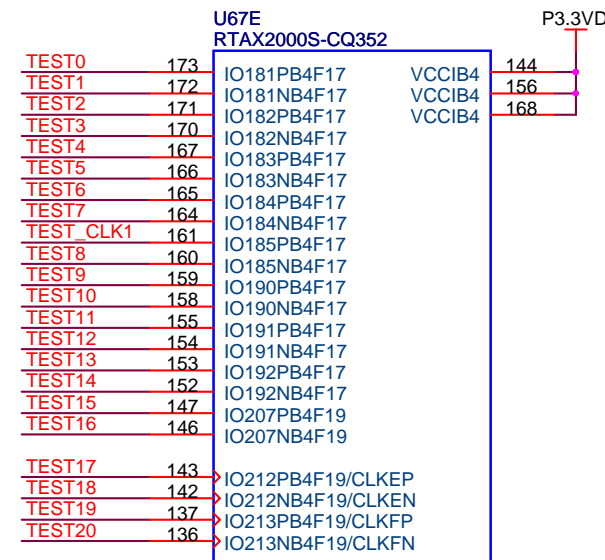
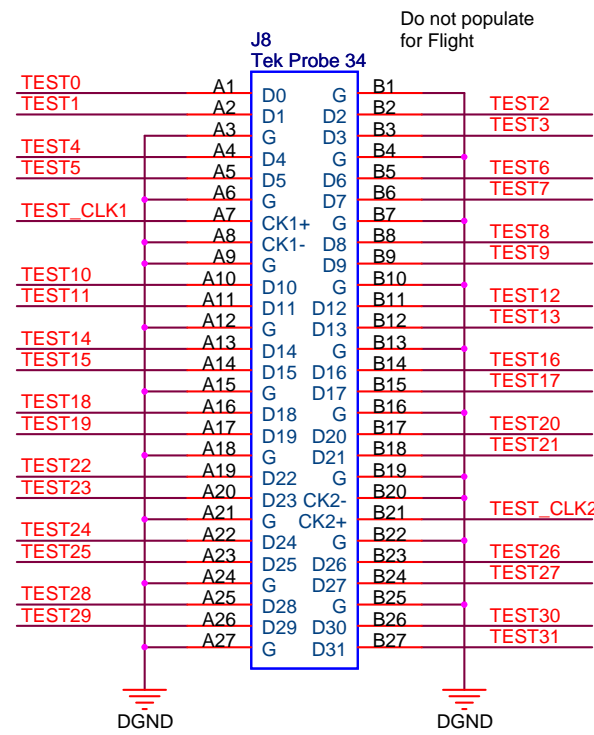
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# FPGA Backplane Interface



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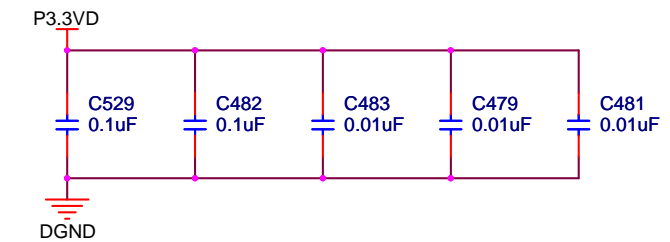
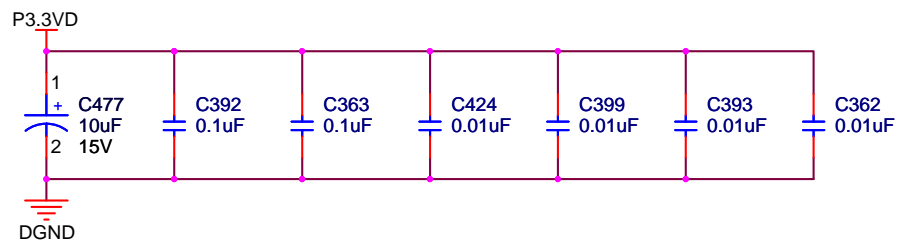
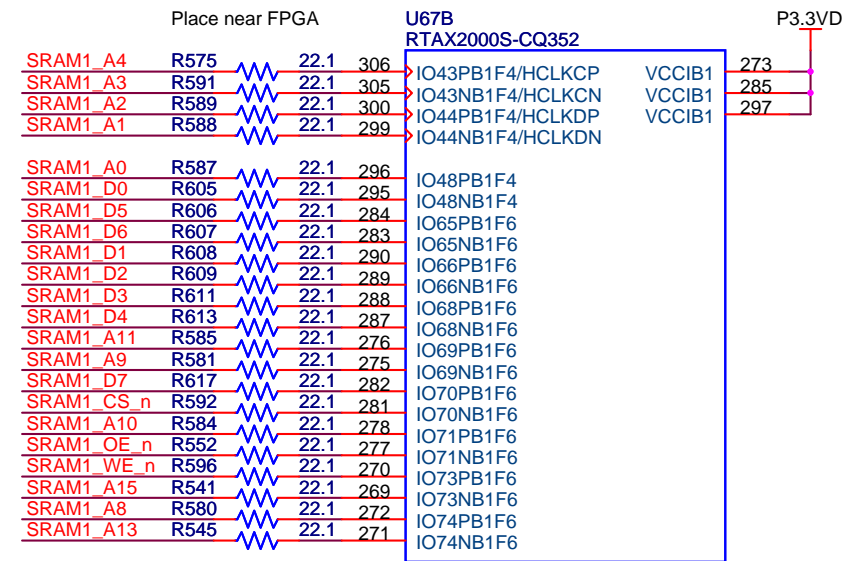
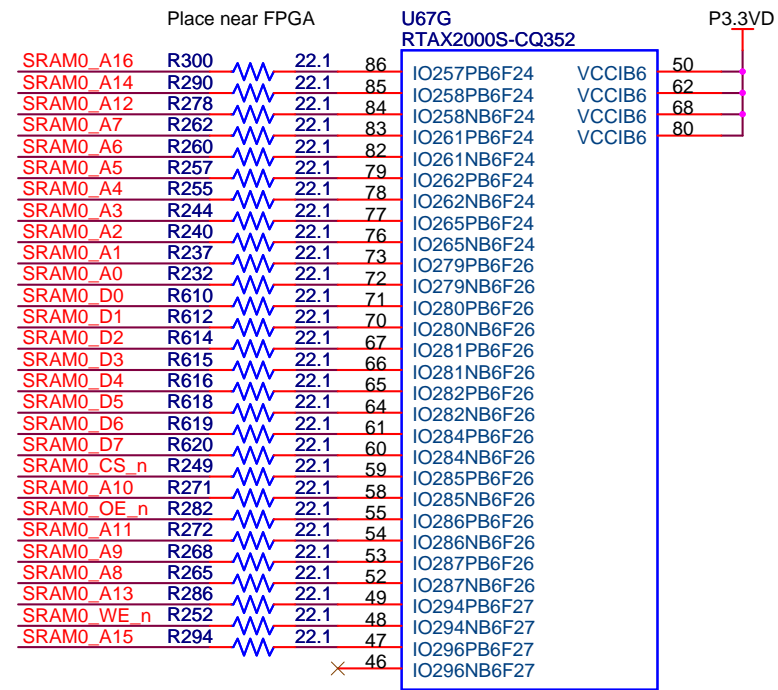
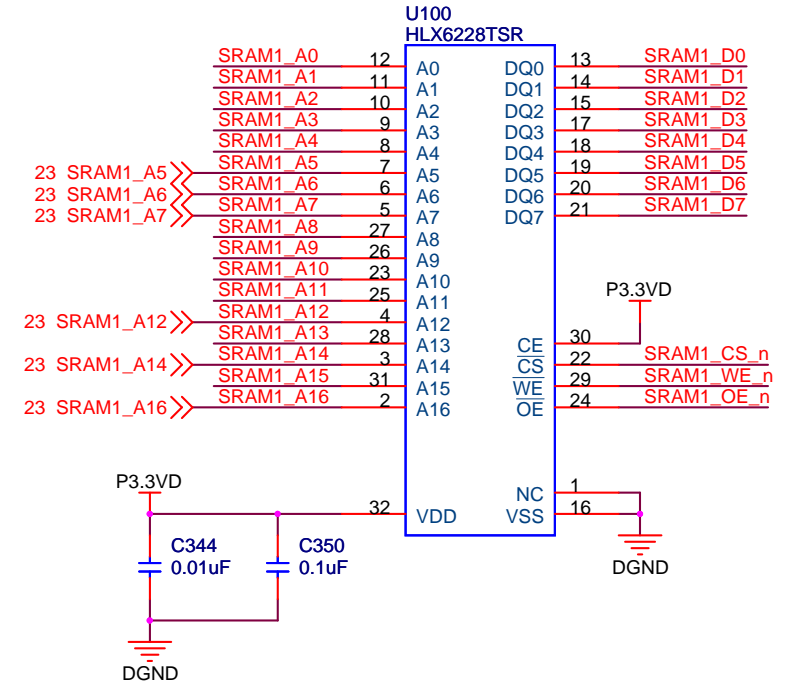
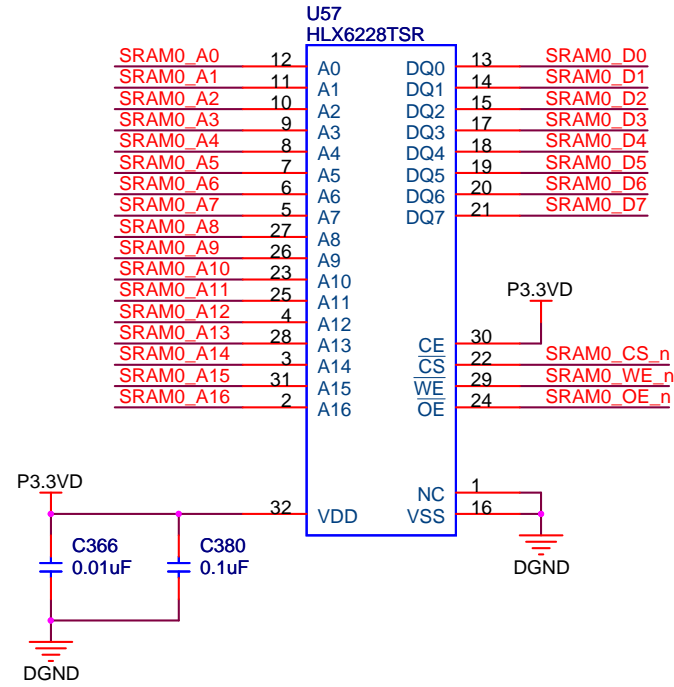
# FPGA Test Probe and LEDs



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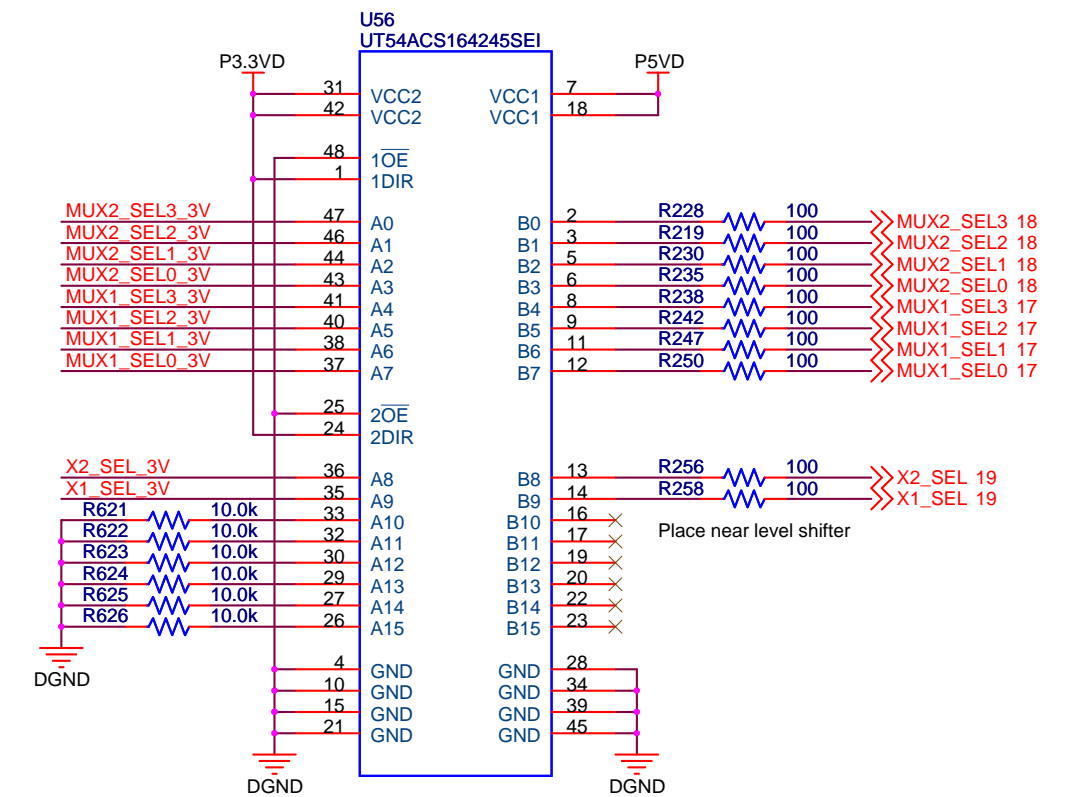
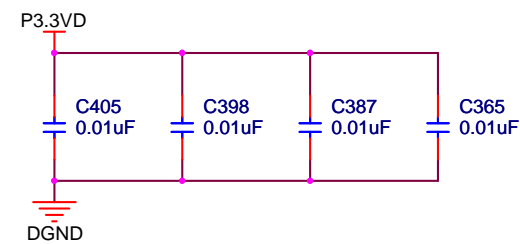
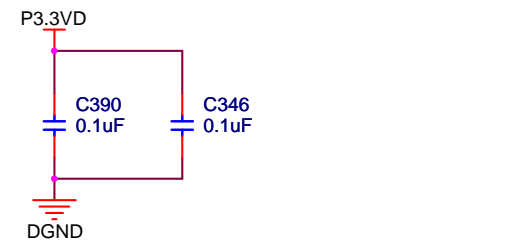
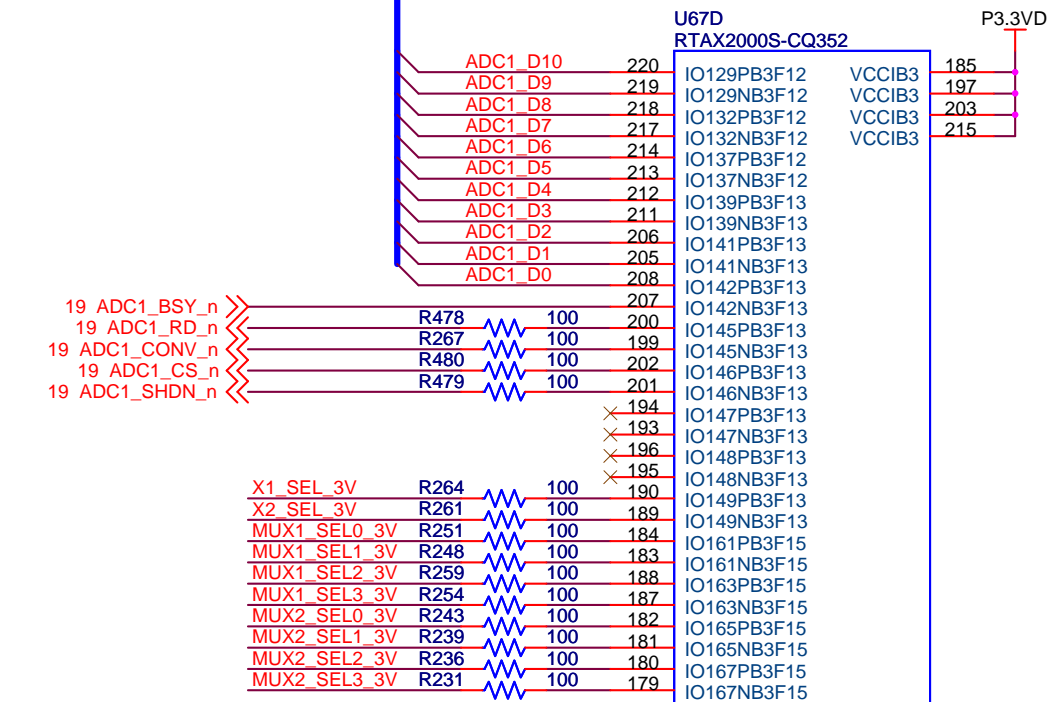
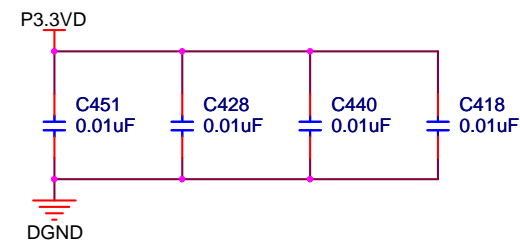
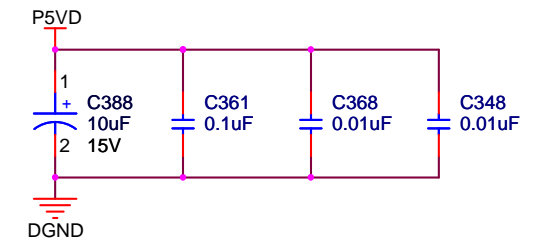
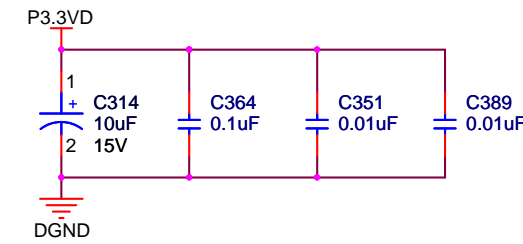
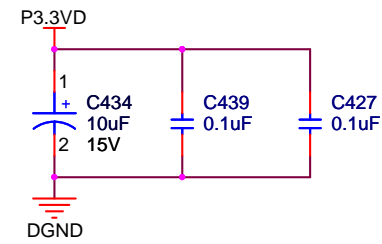
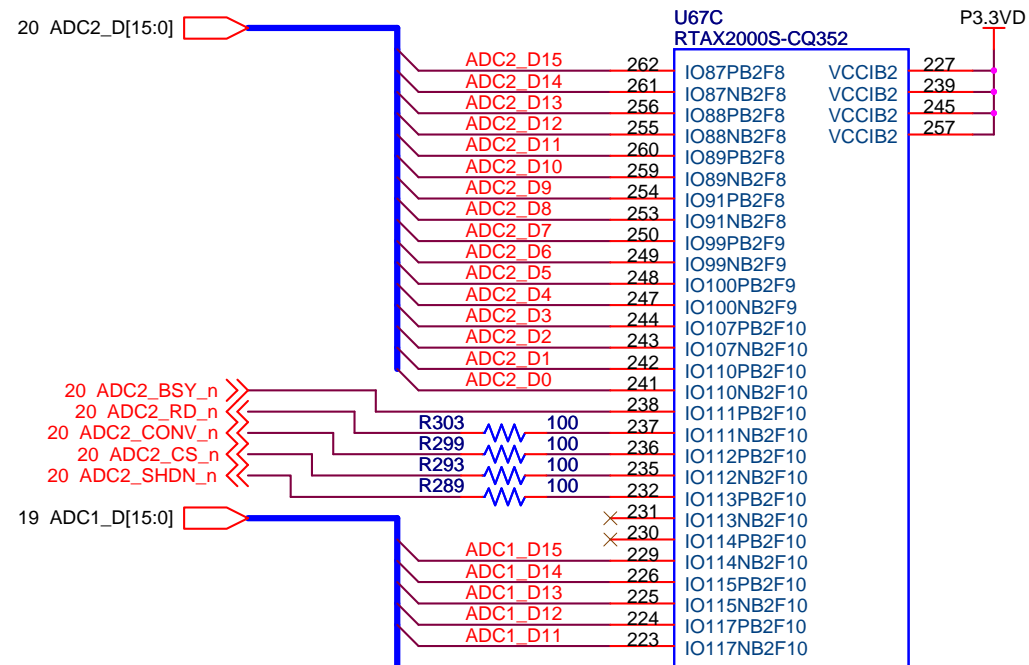


# FPGA SRAM

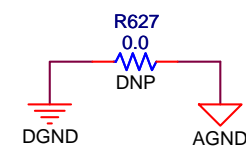


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# FPGA ADC



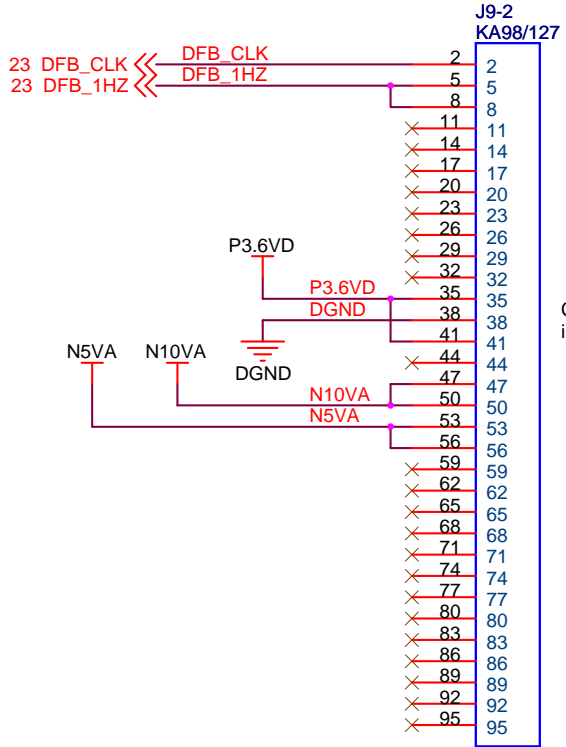
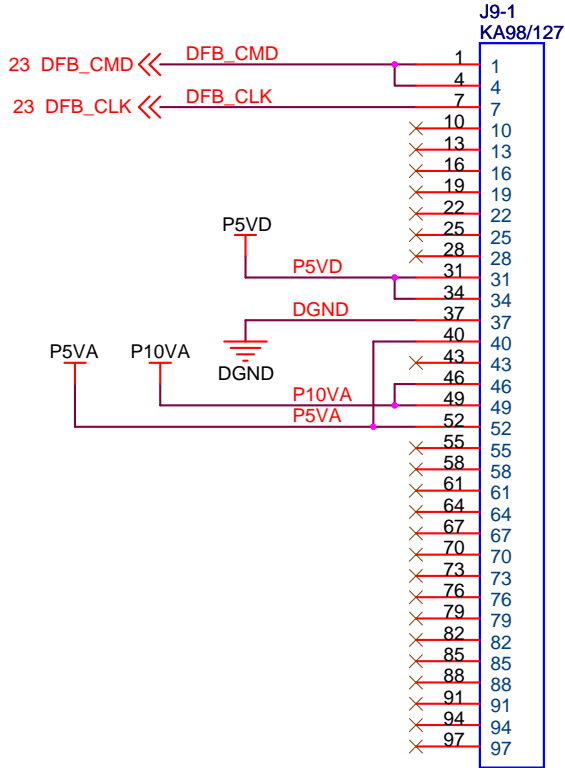
Place near this UT54ACS164245 transceiver



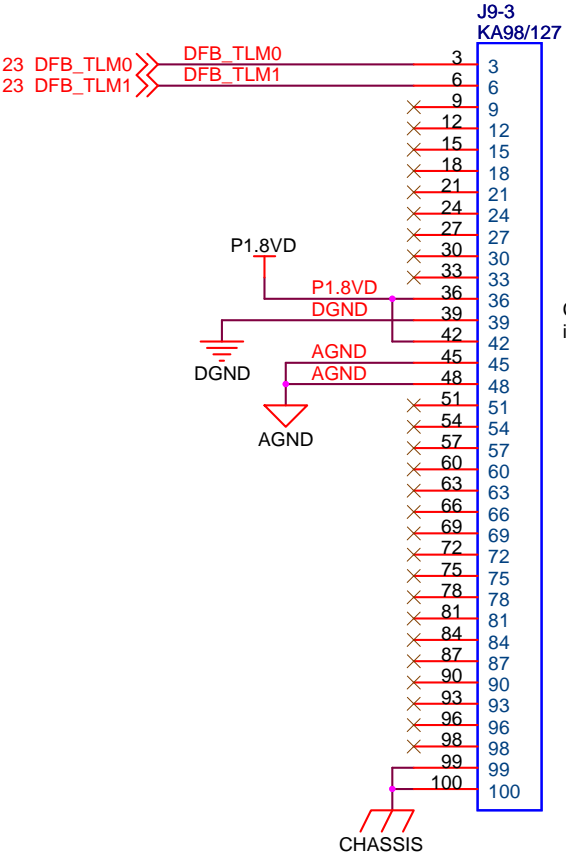
Place near level shifter

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# Backplane Connector

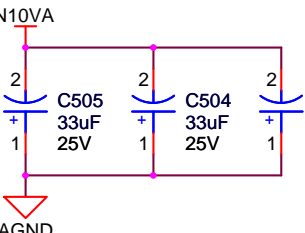
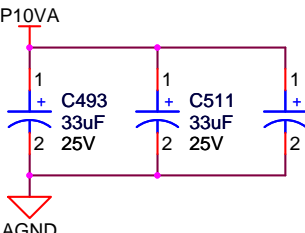
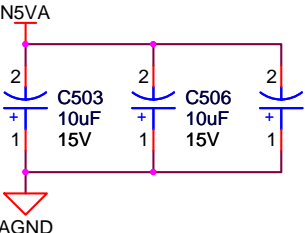
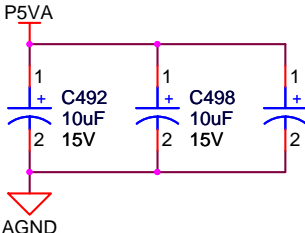
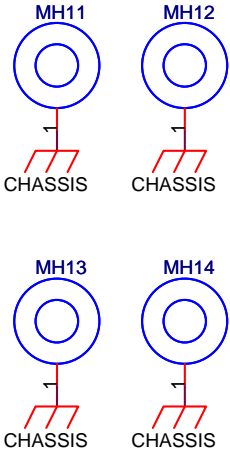


Cut pins 35 and 41 and install inductor L2.

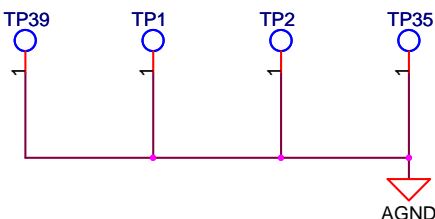
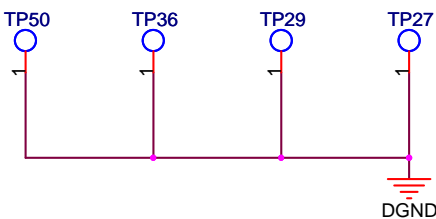
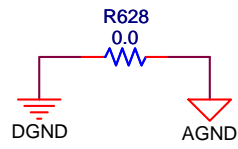


Cut pins 36 and 42 and install inductor L1.

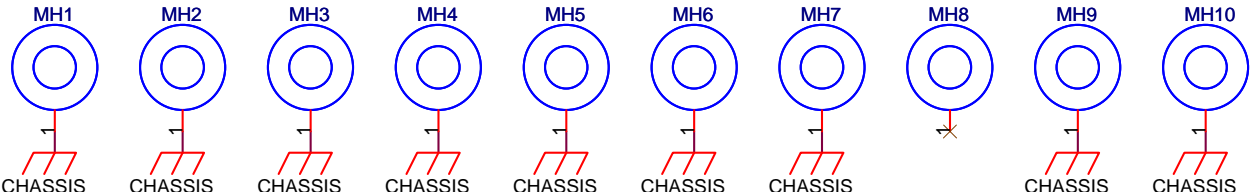
Jackscrew Block Mounting Holes



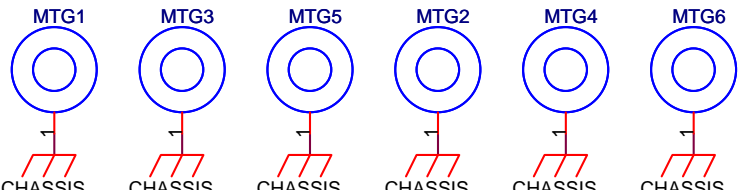
Place near backplane connector



EMI Shield Mounting Holes



Wedglock Mounting Holes



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