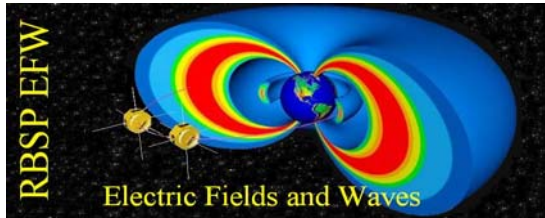


RBSP EFW Digital Control Board (DCB) Specification

RBSP_EFW_DCB_003E_Specification.doc
06/12/2009

Michael Ludlam, U.C. Berkeley RBSP EFW IDPU Engineer

David Curtis, U.C. Berkeley RBSP EFW Systems Engineer



Document Revision Record

Rev.	Date	Description of Change	Approved By
-	5/22/08	Preliminary Draft	-
B	6/27/08	Added Overcurrent Circuit Polarity, removed text more relevant in FPGA or FSW specification	
C	8/8/08	Removed SDRAM and ADC OC protection, amended backplane and corrected S/C connector pinout.	
D	10/20/08	Updated Mux configuration, updated block diagram, power numbers and added MDM 51 debug pinout	
E	6/12/09	New connector and minor edits	

Distribution List

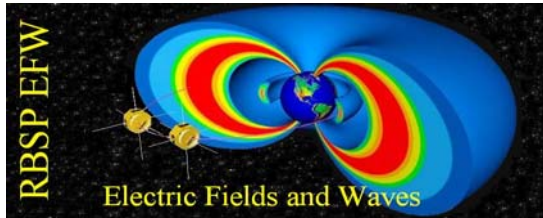
Name	Email (thm_backplane)
Peter Harvey, FSW, UCB	prh@ssl.berkeley.edu
Michael Ludlam, IDPU, UCB	mludlam@ssl.berkeley.edu
Dorothy Gordon, DCB, UCB	dag@ssl.berkeley.edu
David Curtis, EFW Systems Engineer, UCB	dwc@ssl.berkeley.edu
Susan Bastite, DFB Systems Engineer, LASP	susan.bastite@lasp.colorado.edu
Ken Stevens, DFB, LASP	kstevens@efficientlogicdesign.com
Wes Cole, DFB, LASP	wesley.cole@lasp.colorado.edu
Peter Berg, LVPS, UCB	pcb@ssl.berkeley.edu
Jane Hoberman, BEB, UCB	jch@ssl.berkeley.edu
William Rachelson, GSE, UCB	wrachelson@ssl.berkeley.edu
Rachel Hochman, IDPU, UCB	rhochman@ssl.berkeley.edu

TBDs

Identifier	Description

Reference Documents

Doc Number	Title
RBSP_EFW_DCB_001	DCB FPGA Specification
RBSP_EFW_DCB_002	DCB IP Core Document
RBSP_EFW_FSW_001	FSW Specification
APL-7417-9083	EFW ICD
RBSP_EFW_FSW_005	EFW Command and Telemetry Document
RBSP_EFW_BPL_001	EFW IDPU Backplane Specification
RBSP_EFW_SYS_001	EFW Systems Requirements



1 Introduction

This document outlines the Data Controller Board (DCB) for the Electric Field and Waves (EFW) instrument on the Radiation Belt Storm Probes (RBSP) mission. It defines the components and basic functionality of the board. Further details are contained in the FPGA specification (RBSP_EFW_DCB_001) and the Flight Software specification (RBSP_EFW_FSW_001). Two flight boards will be built, along with a spare board (TBD), an engineering board and breadboard.

2 Requirements

The EFW instrument requirements are found in RBSP_EFW_SYS_001. The requirements pertaining to the DCB board are listed below for reference. The up to date list found in RBSP_EFW_SYS_001 remains the master document when referencing requirements. Requirement for the FSW are not listed here.

ID	Req. Title	Subject	Priority	Requirement Body or Section Heading
EFW-81	EFW Command	The EFW IDPU	shall	accept commands via serial interface
EFW-82	EFW Telemetry Rate	The EFW IDPU	shall	generate a continuous, serial telemetry stream at a rate not to exceed 12,000 bps.
EFW-83	EFW Telemetry Peak	The EFW IDPU	shall	limit the instantaneous data rate to the spacecraft to ≤ 80 kbps
EFW-84	EFW Telemetry Compression	The EFW IDPU	shall	perform data compression
EFW-85	EFW use of MET	The EFW IDPU	shall	use Mission Elapsed Time (MET) as the reference time for time stamps produced for science, space weather, and instrument housekeeping data.
EFW-86	EFW MET Acceptance	The EFW IDPU	shall	accept the distribution of MET from its respective spacecraft at a frequency of 1 Hz.
EFW-87	EFW Serial Interface	The EFW IDPU	shall	accommodate a standard point-to-point serial interface for data exchange with the spacecraft.
EFW-92	EFW Engineering Mode	The EFW IDPU	shall	provide an Engineering Mode for deployments
EFW-93	EFW Normal Mode	The EFW IDPU	shall	provide a Normal Mode for science data collection
EFW-94	EFW Burst Mode	The EFW IDPU	shall	provide a Burst Mode for high speed collections
EFW-96	EFW Illegal Commands	The EFW IDPU	shall	validate commands prior to execution.
EFW-97	EFW Data Integrity	The EFW IDPU	shall	detect and correct data errors in its Solid State Recorder.
EFW-133	EFW EMI/EMC Capabilities	The EFW Suite	shall	comply with the requirements and constraints imposed by the RBSP Electromagnetic Environment Control Plan, APL document no. 7417-9018.
EFW-137	EFW Quality Assurance	The EFW Suite	shall	comply with the RBSP Performance Assurance Implementation Plan, as modified by the Compliance Matrix

3 Block Diagram

The DCB board block diagram is shown in figure 1 below.

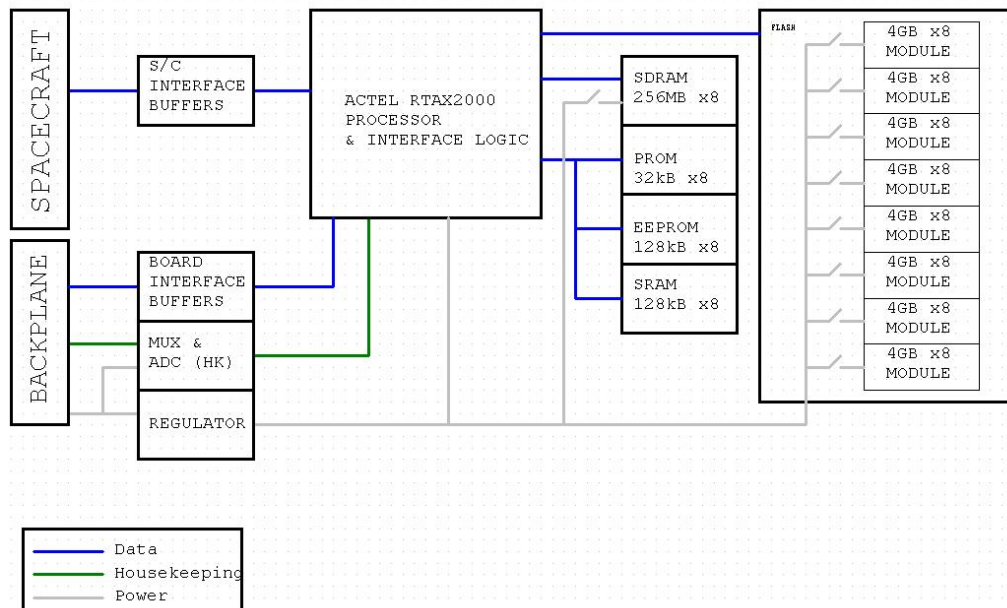
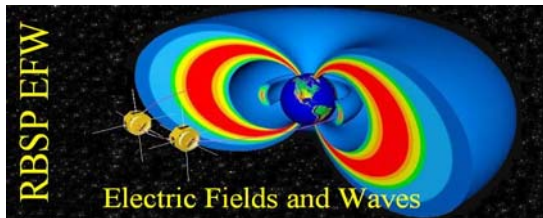


Figure 1: DCB Block Diagram

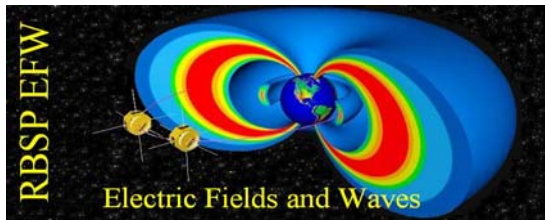
4 Functional Overview

The Data Controller Board (DCB) houses the EFW instrument processor (Z80) inside a RTAX2000S Actel using a CAST Inc IP core. This Actel also houses the control logic that interfaces to the spacecraft, other instrument boards and on card memory. Boot software, stored in PROM (32kB) and patchable EEPROM (128kB) software is based on many UCB EFW instruments including those for THEMIS, FAST and POLAR. Software is copied from PROM and EEPROM to run in SRAM (128kB). The board also has SDRAM (256MB) and Flash Memory (32GB) for storage of science data, and an ADC for digitization of housekeeping quantities.

4.1 Science Data Collection & Transmission

Data is acquired from the Digital Fields Board (DFB) and stored in SDRAM by using DMA channels in the FPGA. Data is packetized here inside 4kB memory segments before being transferred to the spacecraft memory or to flash memory. Survey data is either held in the SDRAM or immediately telemetered to the spacecraft. The Burst data is either held in the SDRAM or stored in the flash memory. The flash memory is composed of 8 parts, each of 4GB that are switched individually to isolate the memory parts from each other and the rest of the DCB circuit. A high signal from the FPGA enables the switch to each device.

When the flash memory is powered to transfer data in or out, the FPGA will take steps to try to ensure that the transfer is completed successfully. Firstly the device will be reset. Data being read from the device will be have data checked using an ECC algorithm with the corresponding



checkbits. These are stored in the flash control bits internal to the flash memory. For write cycles the FPGA will generate the ECC bits and write them to the control bits in the flash memory along with the data, and provide option for post program verification. Data stored in the flash memory is transferred to the SDRAM first if it is to be telemetered to the spacecraft. Data will be compressed here by FSW if necessary before it is sent out on the spacecraft interface. Details of the compression scheme will be found in the FSW specification.

Analog housekeeping values will be digitized by a single ADC. A multiplexer will provide the switched voltages to the ADC that is controlled by the FSW through the FPGA logic. More information is detailed in the ADC section below.

4.2 Memory Buses

There are 4 buses on the board:

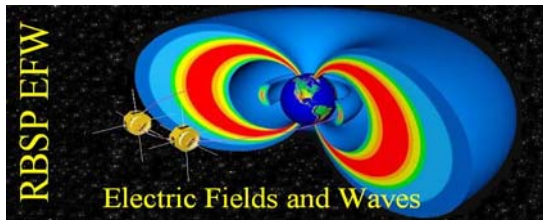
1. CPU Bus
Internal to the FPGA. This is used by the CPU only but interfaces with the memory bus with the FPGA logic acting as bus arbitrator.
2. Memory Bus
PROM, EEPROM, SRAM and the ADC sit on this bus.
3. SDRAM Bus
The SDRAM has it's own private bus that is controller by the FPGA logic.
4. Flash Bus
The Flash memory has it's own private bus that is controlled by the FPGA logic.

4.3 Memory Map

See RBSP_EFW_DCB_001 (FPGA Specification) for details.

4.4 Power

The DCB board requires the following power supplies: +1.8VD, +3.6VD, +5VD, +5VA, -5VA, +10VA, -10VA. Table below shows the breakdown of current consumption by major component. These numbers are estimates and will be updated when current consumption is measured on the breadboard / engineering unit. The 1.8 VD supply will be regulated down to 1.5VD for the Actel. The 3.6VD supply will be regulated down to 3.3VD. Where there is a current protection switch an LDO will also be implemented for that supply. See section below on current protection.



Component	Manufacturer	Part No	Quantity	Supply (V)	Peak Icc (mA)	Avg Icc(mA)	Peak Total (mW)	Average Total (mW)
FPGA	Actel	RTAX2000S	1	3.3	27	24	90	80
FPGA	Actel	RTAX2000S	1	1.5	373	187	560	280
Prom	BAE	238A790	1	3.3	19	0	63	0
EEProm	Maxwell	28LV010	1	3.3	25	0	84	0
SRAM	Honeywell	HLX6228	1	3.3	36	36	120	120
SDRAM	3d-Plus	MMSD08256804S-C-1S	1	3.3	200	50	660	165
Flash	3d-Plus	MMFN08408808S-F-1S	8	3.3	40	0	132	0
Buffers	Aeroflex	UT54ACS164245SEI	18	3.3	10	5	297	149
ADC	Linear	LTC1604	1	5	18	1	90	5
ADC	Linear	LTC1604	1	-5	26	1	130	5
Mux	Intersil	HI-0508	1	10	1	0.5	10	5
Mux	Intersil	HI-0508	1	-10	1	0.5	10	5
LVDS Receiver	Aeroflex	UT54LVDS032LV	1	3.3	15	15	50	50
LVDS Driver	Aeroflex	UT54LVDS031LV	1	3.3	18	18	59	59

Total Power		2236	923
Total 3.3V Current	391	149	
Total 1.5V Current	373	187	

Regulator Power Disipation		
3.3V in mW	117.4	44.6
1.5 in mW	112.0	56.0

5 Component Description

5.1 Processor

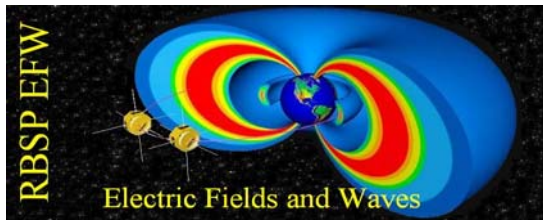
The DCB uses a IP core implementation of a Z80 processor inside an Actel RT2000S FPGA. The core, from CAST Inc, will run at 16.777MHz (2^{24} Hz) driven by an on card oscillator. A full description of the core is contained in RBSP_EFW_DCB_002.

5.2 Actel FPGA

The Actel FPGA is a 352 pin CQFP RTAX2000S part. For the breadboard a commercial AP1000S reprogrammable part is used instead. The engineering board will use the Aldec board that has an Actel A3EP1500 part on an adaptor board that fits the CQFP-352 footprint of the flight part. A prototype RTAX2000S will be used once the design is sufficiently mature. The external oscillator clocks the FPGA logic that glues the processor with the memory and external interfaces at the same frequency as the processor. A full description of the FPGA specification is described in RBSP_EFW_DCB_001.

5.3 Spacecraft Interface

The DCB board provides the digital interface to the spacecraft, receiving commands and sending science and housekeeping telemetry. The protocol for this is LVDS, using Aeroflex parts UT54LVDS031LV and UT54LVDS032LV to drive the interface. The breadboard DCB uses the same driver parts as on the APL provided GSE (TI pn#SN65LVDM176). The six line interface comprises of three differential signals – command, telemetry and 1Hz/SpinPulse. The command and telemetry interface run at 115.2 kbaud. Commands can be received at any time during the first 950 ms after the 1Hz tick. Telemetry can be sent at any time in the first 950 ms after the 1Hz tick. More detailed information is contained in the EFW ICD (APL Document 7417-9083).



5.4 Reset

A power on reset (POR) circuit provides a global board reset signal to the FPGA. The FPGA should double clock the active low signal before triggering a reset. The POR is Or'd together with a watchdog reset register inside the FPGA. If the software does not write to the watchdog register every 3 seconds a reset will be triggered. The watchdog can be disabled using an external FPGA pin tied to ground. A FSW command resets the FSW only – and is detailed in the FSW specification (RBSP_EFW_FSW_001).

5.5 PROM

The flight board has a single 32k x 8bit PROM memory from BAE Systems (pn#238A790). This will store the standard boot FSW code. Both parts are housed in a 28 pin flatpack package. For the breadboard design the prom will be replaced by a 128k x 8 EEPROM (ATMEL pn#AT28LV010) that can be programmed via the serial interface provided or via the spacecraft interface once boot code is running. Jumpers on the breadboard provide for segmentation of the device into 4 blocks. The engineering board is likely to have a socket for both the dual inline packaged EEPROM (AT28BV256) and the flatpack PROM. Initial board testing will be done with the EEPROM, which will be replaced with the programmed PROM part when FSW is ready. Note that to program the 3.3V Atmel EEPROM a security code is required to unlock the device (i.e. the write protect function is always enabled).

5.6 EEPROM

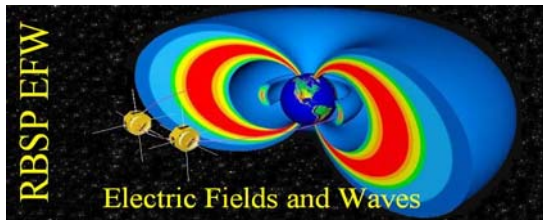
A 128k x 8bit EEPROM from Maxwell will provide space for patches and storage of instrument configuration scripts (pn#28LV010). For the breadboard the ATMEL equivalent part will be used (pn#AT28LV010). The part for the engineering model is the engineering version of the Maxwell part.

5.7 SRAM Memory

The flight board will have a single 128k x 8 SRAM part from Honeywell (pn#HLX6228). The breadboard uses an equivalent 128k x 8 part from ISSI (pn#IS62WV1288BLL). The part for the engineering model is the engineering version of the Honeywell part.

5.8 Serial Flash

There is the option to install a serial flash 64k x 8 part on the breadboard (ST pn#M25P05A). This would allow up or down load of data via a SPI USB interface to a PC using a dediprogram device (<http://www.dediprogram.com/product.php?UID=2>).



5.9 SDRAM

A single 256MByte SDRAM module provides the storage for telemetry from the DFB before it is telemetered to the spacecraft or stored in the Flash memory. The part (3d-Plus pn#MMSD08256804S-C) operates on a single 3.3V switched supply. The part meets the latch up requirement and therefore does not need an overcurrent protection circuit. However the part does have a power switch for flexibility. The SDRAM resides on a private memory bus that is buffered (TBD).

5.10 Flash Memory

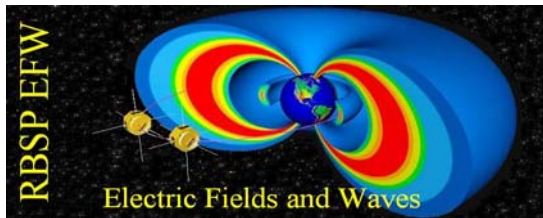
Eight 32Gbit NAND Flash memory parts are used for storage of burst telemetry data. The parts are 50 pin SOP packaged parts, that have 3 Vcc (3.3V) pins and 4 ground pins. 8 I/O pins are used to transfer data and commands and the other pins provide control to the device. As the flash memory has a relative high incidence of SEFI and SEU effects (see proton affects TN16) it is recommended to keep the parts unpowered except when a read or write to the device occurs. Each flash parts will require 1 ½ 16 bit buffers, 1 buffer drives the chip enable (CE) pins and other control signals and the other buffer drives the I/O pins for two flash modules. The flash memory will be powered on writing to a register in the FPGA. Although flash memory can be programmed bit by bit it is much more efficient to program it in pages (2kB) or blocks (128kB).

5.11 ADC

A single LTC1604 ADC provides the digitalization of analog housekeeping for the instrument. The BEB and PCB housekeeping lines are multiplexed with the DCB housekeeping signals into the ADC. Table 1 provides the Analog HK decoding on the DCB. All inputs shall be between -2.5V and +2.5V. The digital side of the ADC sits on the memory bus (MEMBUS) controlled by the FPGA. The conversion time is controlled by a write to a register in the FPGA and the data is made available at address 0x40000 after conversion (see memory map for details). The ADC requires +5VA, +5VD and -5VA.. To conserve power the ADC should kept in nap mode when the CPU is not requesting a conversion. The CPU should allow 500us for the voltage to settle at the output of the analog mux following a channel switch prior to performing a conversion.

MUX	HK Name	HK Function
0	PCB_HK	PCB Housekeeping Line
1	BEB_HK	BEB Housekeeping Line
2	TEMP_FPGA	FPGA Temperature
3	P33VD	3.3V Voltage Monitor
4	P33IMON	3.3V Current Monitor
5	P15VD	1.5V Voltage Monitor
6	P15IMON	1.5V Current Monitor
7	DGND	Digital Ground

Table 1



5.12 Current Protection Circuit and Low Dropout Regulator

There is no hardware controlled current protection for any individual DCB component. The 3.6VD and 1.8VD supplies have current monitors that are available for sampling by the FSW.

A radiation hardened LDO regulator is implemented on the 3.6VD and 1.8VD supplies from MS Kennedy (part number MSK5822-3.3RH and MSK5822-1.5RH).

5.13 Backplane Interface

The DCB communicates with the DFB using an all 3.3V interface. 3.3V 54AC14 devices provide buffering to the backplane. The DCB sends commands to the DFB and receives science and housekeeping telemetry. The DCB also communicates with the LVPS/PCB and the BEB boards using a 5V interface. Aeroflex part UT54ACS164245SEI provides the level shifting and buffering to these two boards. More details about the interface can be found in the RBSP EFW backplane specification (RBSP_EFW_BPL_001).

The BEB requires a series of DAC commands to be sent to the board when DAC settings are changed. There are 20 DAC commands in total and they are stored in registers in the DCB FPGA. FSW writes to a register in the FPGA to send the commands to the BEB. More information is contained in the DCB FPGA specification (RBSP_EFW_DCB_001).

5.14 Buffers

Where necessary the following device will be used on the flight board. <http://ams.aeroflex.com/ProductFiles/DataSheets/MSI/msi16245SSEI.pdf> This provides level shifting (from 3.3V to 5V) and buffering of signals to memory, ADC and the backplane where necessary.

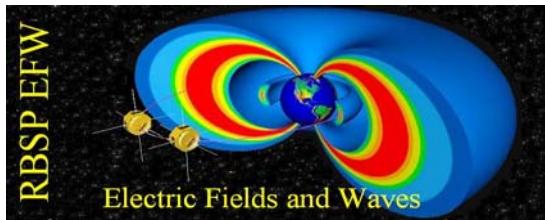
5.15 Debug Board

A separate debug board is used for check out and FSW testing of the DCB board. It contains a EEPROM, switches, LEDs and Logic Analyzer connections. The as built schematic is drawing number RBSP_EFW_DCB_005C.

6 Layout requirements

The DCB circuit is populated on a 6U VME card. The highest component is the 3d-Plus Flash memory module (11.93mm high). The envelope for the components on the card is detailed in the backplane specification (RBSP_EFW_BPL_001). IC components will go on the top of the board, passive components on the bottom.

The board mechanical drawing (RBSP-IDP-MEC-011 REV F DCB PCB OUTLINE.pdf) shows keep out areas and spacing of connectors and mounting holes.



7 Connectors

The DCB has three connectors. One connects to the Spacecraft, one to the other IDPU boards and the other is used for debugging and test and is not connected after instrument delivery to APL.

7.1 Spacecraft Data Interface

The DCB connects to the spacecraft C&DH via a single 9 pin D male sub connector. The pin out is listed in Table 2 below. The protocol for communication with the spacecraft is listed in the EFW ICD (APL-7417-9083).

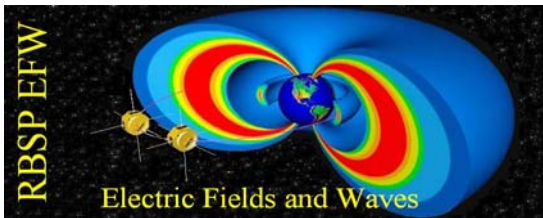
Pin #	Signal Name	Signal Function
1	1PS/SP_P	1Hz & Sun Pulse Positive
2	-	NC
3	TC_N	Telecommand Negative
4	TLM_P	Telemetry Positive
5	DGND	Digital Ground
6	1PS/SP_N	1Hz & Sun Pulse Negative
7	TC_P	Telecommand Positive
8	-	NC
9	TLM_N	Telemetry Negative

Table 2: S/C Connector pin out

7.2 Backplane Power & Data Interfaces

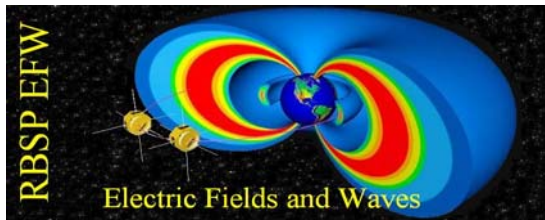
The DCB communicates with the other IDPU boards via the backplane. It also receives power from the LVPS/PCB board on the same connector. The pins used on the backplane connector are listed in Table 3 below. The connector is a Hypertronics KA98/127 style connector.

BKP Pin #	Signal Name	Signal Function
1	DFB_CMD	DFB Command
2	DFB_CLK	DFB Clock
3	DFB_TLM0	DFB Telemetry Line0
4	DFB_CMD	DFB Command
5	DFB_1HZ	DFB 1Hz
6	DFB_TLM1	DFB Telemetry Line1
7	DFB_CLK	DFB Clock
8	DFB_1HZ	DFB 1Hz
9	DIG_SPARE9	Spare
10	PCB_CMD	PCB Command
11	DIG_SPARE11	Spare
12	BEB_ACTEST2	BEB Actest Line2



13	DIG_SPARE7	Spare
14	DIG_SPARE8	Spare
15	BEB_ACTEST1	BEB Actest Line1
16	BEB_AMUX_EN0	BEB Analog Mux Enable0
17	BEB_AMUX_EN1	BEB Analog Mux Enable1
18	BEB_AMUX_EN2	BEB Analog Mux Enable2
19	BEB_AMUX_A0	BEB Analog Mux Address0
20	BEB_AMUX_A1	BEB Analog Mux Address1
21	BEB_AMUX_A2	BEB Analog Mux Address2
22	BEB_DAC_CMD	BEB DAC Command
23	BEB_DAC_CLK	BEB DAC Clock
24	BEB_DAC_LDAC	BEB DAC Load DAC
25	BEB_DAC_CS	BEB DAC Chip Select
26	PCB_CLK	PCB Clock
27	PCB_STB	PCB Strobe
28	PCB_CMD	PCB Command
29	PCB_CLK	PCB Clock
30	PCB_STB	PCB Strobe
31	IDPU_P5VD	IDPU +5VD
32	LVPS_CLOCK	LVPS Converter Clock
34	IDPU_P5VD	DCB & DFB +5VD
35	IDPU_P3.6VD	DCB & DFB +3.6VD
36	IDPU_P1.8VD	DCB & DFB +1.8VD
37	IDPU_DGND	DCB & DFB Digital Ground
38	IDPU_DGND	DCB & DFB Digital Ground
39	IDPU_DGND	DCB & DFB Digital Ground
40	IDPU_P5VA	IDPU_P5VA
41	IDPU_P3.6VD	IDPU_P3.6VD
42	IDPU_P1.8VD	IDPU_P1.8VD
45	IDPU_AGND	DCB & DFB Analog Ground
46	IDPU_P10VA	IDPU +10VA
47	IDPU_N10VA	IDPU -10VA
48	IDPU_AGND	DCB & DFB Analog Ground
49	IDPU_P10VA	DCB & DFB +10VA
50	IDPU_N10VA	DCB & DFB -10VA
51	BEB_ANALOG_HKP	BEB Analog HK
52	IDPU_P5VA	DCB & DFB +5VA
53	IDPU_N5VA	DCB & DFB -5VA
54	PCB_ANALOG_HKP	PCB Analog HK
56	IDPU_N5VA	IDPU -5VA

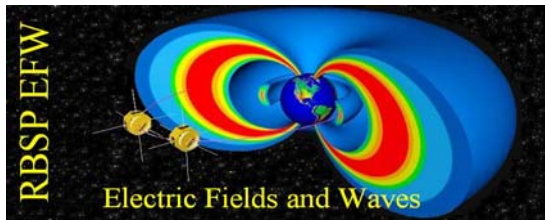
Table 3: Backplane Interface Connections



7.3 Debug Interface

The Breadboard DCB contains all the debugging connections on the board through numerous 20 pin headers surrounding the Actel FPGA part. The engineering and flight units will not have these headers on the board. There will be a single MDM 51S connector that provides an interface to a debug board that can be connected while the board is installed in the IDPU chassis.

MDM Pin #	Signal Name
1	DGND
2	MEMADDR0
3	MEMADDR1
4	MEMADDR2
5	MEMADDR3
6	MEMADDR4
7	MEMADDR5
8	MEMADDR6
9	MEMADDR7
10	MEMADDR8
11	MEMADDR9
12	MEMADDR10
13	MEMADDR11
14	MEMADDR12
15	MEMADDR13
16	MEMADDR14
17	MEMADDR15
18	MEMADDR16
19	MEMDATA0
20	MEMDATA1
21	MEMDATA2
22	MEMDATA3
23	MEMDATA4
24	MEMDATA5
25	MEMDATA6
26	MEMDATA7
27	DGND
28	MBUSCYTYPE0
29	MBUSCYTYPE1
30	MBUSCYTYPE2
31	MBUSCYTYPE3
32	MISCCTRL0
33	MISCCTRL1
34	MISCCTRL2



35	MISCCTRL3
36	MISCCTRL4
37	MISCCTRL5
38	MISCCTRL6
39	MISCCTRL7
40	MISCCTRL8
41	MISCCTRL9
42	MISCCTRL10
43	MISCCTRL11
44	LASTROBE0
45	LASTROBE1
46	LASTROBE2
47	NMI
48	DEBUG_nRESET
49	RxD
50	TxD
51	P3.3VD

8 Commands

Commands are contained in the command and Telemetry document RBSP_EFW_FSW_005_CTM.